MC92603 Quad Gigabit Ethernet Transceiver Reference Manual

MC92603RM
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freescale™
semiconductor

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About This Book

The primary objective of this reference manual is to describe the functionality of the MC92603 for software and hardware developers.

Information in this book is subject to change without notice, as described in the disclaimers on the title page of this book. As with any technical documentation, it is the readers' responsibility to be sure they are using the most recent version of the documentation.

Audience

It is assumed that the reader has the appropriate general knowledge regarding the design and layout requirements for high-speed (Gbps) digital signaling and understanding of the basic principles of the Ethernet and Fibre Channel communications protocols to use the information in this manual.

Organization

The following is a summary and a brief description of the major chapters in this manual:

- Chapter 1, "Introduction," gives an overview of the device features and shows a block diagram of the major functional blocks of the part.
- Chapter 2, "Transmitter," describes the MC92603 transmitter, its interfaces, and operational options.
- Chapter 3, "Receiver," gives a description of the receiver, its interfaces, and operation.
- Chapter 4, "Management Interface (MDIO)," describes the MDIO interface signals and the associated registers.
- Chapter 5, "System Design Considerations," describes the system considerations for the MC92603, including clock configuration, device startup and initialization, and proper use of the configuration control signals.
- Chapter 6, "Test Features," covers the JTAG implementation and the system accessible test modes.
- Chapter 7, "Electrical Specifications and Characteristics," describes the DC and AC electrical characteristics.
- Chapter 8, "Package Description," provides the package parameters and mechanical dimensions and signal pin to ball mapping tables for the MC92603 device.
- Appendix A, "Ordering Information," provides the Freescale part numbering nomenclature for the MC92603 transceiver.
- Appendix B, "8B/10B Coding Scheme," provides tables of the fibre channel-specific 8B/10B encoding and decoding as based on the ANSI FC-1 fibre channel standard.

- Appendix C, "Revision History," lists the major differences between revisions of this book, the *MC92603 Quad Gigabit Ethernet Transceiver Reference Manual* (MC92603RM).
- "Glossary of Terms and Abbreviations," contains an alphabetical list of terms, phrases, and abbreviations used in this book.
- "Index," contains all general entries for the book.

Suggested Reading

This section lists additional reading that provides background for the information in this manual as well as general information about the architecture.

General Information

The following documentation, published by Morgan-Kaufmann Publishers, 340 Pine Street, Sixth Floor, San Francisco, CA, provides useful information about the PowerPC™ architecture and computer architecture in general:

- *The PowerPC Architecture: A Specification for a New Family of RISC Processors*, Second Edition, by International Business Machines, Inc.
- *Computer Architecture: A Quantitative Approach*, Second Edition, by John L. Hennessy and David A. Patterson
- *Computer Organization and Design: The Hardware/Software Interface*, Second Edition, David A. Patterson and John L. Hennessy

Related Documentation

Freescale documentation is available from the sources listed on the back cover of this book; the document order numbers are included in parentheses for ease in ordering:

- Reference manuals—These books provide details about individual device implementations. The *MC92603DVB Quad GEt Design Verification Board User's Guide* (MC92603DVBUG) describes how to use the design verification board and should be read in conjunction with this manual, the *MC92603 Quad Gigabit Ethernet Transceiver Reference Manual* (MC92603RM). An applications evaluation kit is also available for the MC92603. Its operation is covered in the *MC92603 Evaluation Kit User's Guide* (MC92603EKVUG).
- Addenda/errata to reference manuals—Because some devices have follow-on parts an addendum provides any additional features and functionality changes. These addenda are intended for use with the corresponding reference manuals.
- Hardware specifications—Hardware specifications provide specific data regarding bus timing, signal behavior, and AC, DC, and thermal characteristics, as well as other design considerations. This manual contains all the hardware specifications for the MC92603.
- Application notes—These short documents address specific design issues useful to programmers and engineers working with Freescale devices.
- White papers—These documents provide detail on a specific design platform and are useful to programmers and engineers working on a specific product. The *MC92610 3.125 Gbaud Reference*

Design Platform (BR1570) describes the technical design process used in developing a high-speed backplane reference design.

- Additional literature is published as new processors become available. For a current list of documentation, refer to http://www.freescale.com.

Conventions

This document uses the following notational conventions:

	Book titles in text are set in italics
	Internal signals are set in italics, for example, *loopback_data*
*	Notation for multiplication
0x	Prefix to denote hexadecimal number
0b	Prefix to denote binary number
x	In some contexts, such as signal encodings, an un-italicized x indicates a don't care.
x	An italicized *x* indicates an alphanumeric variable.
n	An italicized *n* indicates a numeric variable.

Signals

A bar over a signal name indicates that the signal is active low—for example, $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$. Active low signals are referred to as asserted (active) when they are low and negated when they are high. Signals that are not active low, such as XMIT_A_ENABLE and DROP_SYNC, are referred to as asserted when they are high and negated when they are low.

Chapter 1
Introduction

This chapter consists of the following sections:

This reference manual explains the functionality of the MC92603 Quad Gigabit Ethernet transceivers (GEt) and enables its use by software and hardware developers. The audience for this publication, therefore, consists of hardware designers and application programmers who are building data path switches and high-speed backplane intercommunication applications.

1.1 Overview

The Gigabit Ethernet transceiver was designed with the intent to meet the requirements of **IEEE Std. 802.3—2002**®. It was designed to fully support full-duplex GMII or TBI PHY applications including the reduced RGMII or RTBI defacto interfaces. Each channel also has its own independent MDIO register set as specified in the above standard.

The MC92603 GEt is designed as four parts in one. It may be configured as either a 1 Gigabit backplane serializer/deserializer (SerDes) with functionally similar to the *1.25 Gbaud Quad SerDes* (MC92600), or as a Quad 1 Gigabit Ethernet PHY and the reduced interface versions of these two.

The GEt is a high-speed, full-duplex, serial data interface device that can be used to transmit data between chips across a board, through a backplane, or through cabling, as well as to interface to GBIC/SFP modules. The multi-channel device has transceivers that transmit and receive coded data at a rate of 1.0 Gbps through each 1.25 gigabaud link.

The MC92603 is built on the proven transceiver technology of the MC92600 and MC92602 devices. Carefully designed for low-power consumption, its CMOS implementation nominally consumes less than 1 W with all links operating at full speed when in the backplane interface mode.

The MC92603 features transmit FIFOs and source synchronous transmit clocks per channel to further simplify interfacing. Additionally, **IEEE Std 1149.1—1990™** JTAG boundary scan and built-in PRBS generator/analyzers are provided for board test support.

1.2 Features

The MC92603 has two applications-oriented operating modes depending on the configuration. It may be used as a backplane SerDes or an Ethernet PHY.

The main features of the MC92603 are as follows:

- Common features:
  - Four independent SerDes channels with full-duplex differential data links
  - Configurable as a dual channel device to provide redundant transmit and receive serial links
  - Selectable speed range: 1.25 or 0.625 Gbaud
  - Internal 8B/10B encoder/decoder that may be bypassed
  - Source synchronous parallel data input interfaces
  - Selectable: source-aligned or source-centered timing on the receiver output interfaces
  - DDR (RGMII/RTBI), source synchronous, 4-/5-bit optional interfaces
  - Parallel interfaces may be either 2.5- or 3.3-V LVTTL. Device will inter-operate with SSTL_2 with the 2.5-V LVTTL interface.
  - Transmit data clock is selectable between per-channel transmit clock or channel ‘A’ transmit clock
  - Received data may be clocked to the reference clock or to the received data frequencies
  - Unused transceiver channel may be disabled
  - Drives 50- or 75-Ω media (100- or 150-Ω differential) for lengths of up to 1.5 meters board/backplane, or 10 meters of coax.
  - Tolerates a $\pm$250 ppm frequency offset between the transmitter and receiver
  - Link inputs have on-chip receiver termination and are ‘hot swap’ compatible
  - Low power (less than 1.0 W) under typical conditions while operating in backplane mode with all transceivers at full speed
  - Differential LVPECL reference clock input with single-ended LVCMOS input option
  - Two single-ended buffered reference clock outputs to be used as the clock source for associated MAC interface logic.
  - Built-in, at speed, self test for production testing and on-board diagnostics
  - IEEE Std. 1149.1 JTAG boundary scan test support
- Backplane application features:
  - Link-to-link synchronization supports aligned, multi-channel word transfers. Synchronization mechanism tolerates up to 40 bit-times of link-to-link media delay skew.
  - Supports disparity-based word sync events for compatibility with legacy transceivers
  - Selectable COMMA code group alignment mode enables aligned or unaligned transfers
- Ethernet friendly features:
  - GMII, TBI, RGMII, or RTBI data interface options
  - COMMA code group alignment in receivers
  - Provides the PCS and PMA layers for Ethernet PHYs as specified in IEEE Std. 802.3-2000
  - MDIO slave interface and registers as defined in IEEE Std. 802.3-2002 are fully supported
  - Supports rate adaption within IPG for jumbo frames up to 14 Kbytes

1.3 Block Diagram

The MC92603 is a highly integrated device containing all of the logic needed to facilitate the application and testing of a high-speed serial interface. No external components, other than the normal power supply decoupling network, are required.

A simplified block diagram of the MC92603 device is shown in Figure 1-1, and a full block diagram is provided in Figure 1-2.

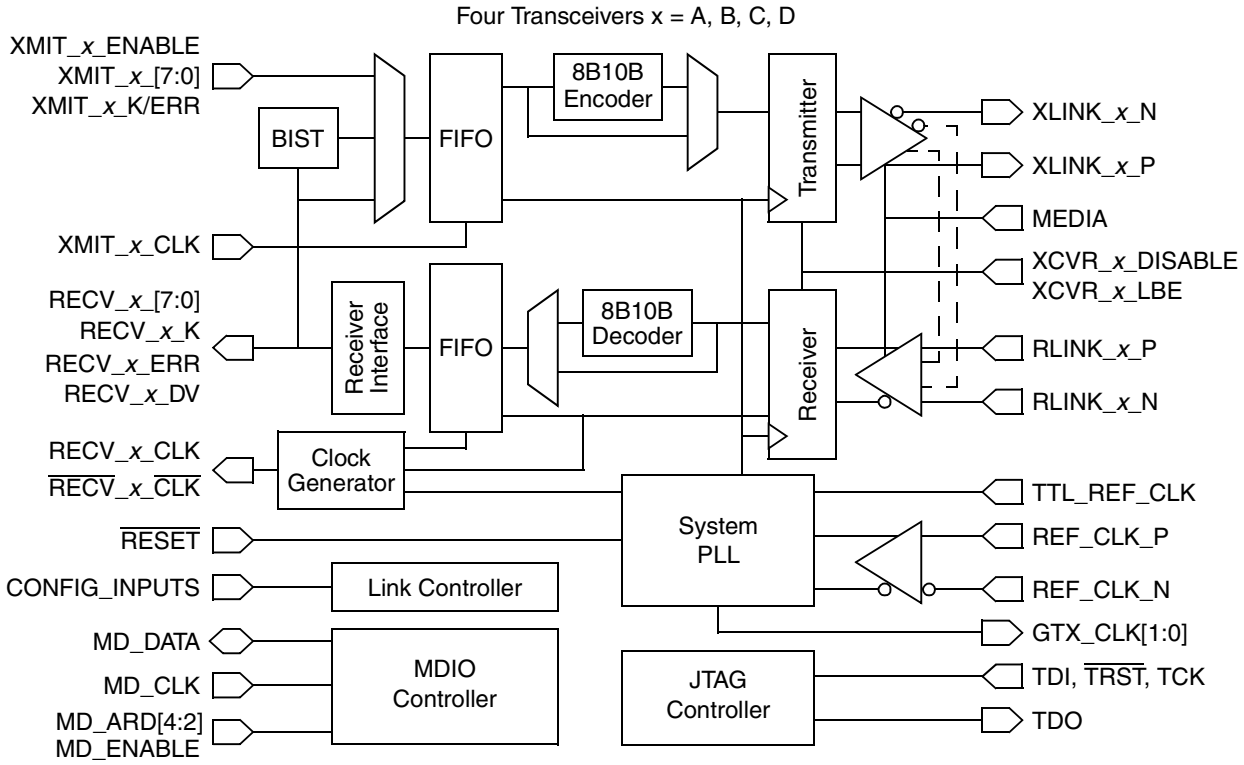
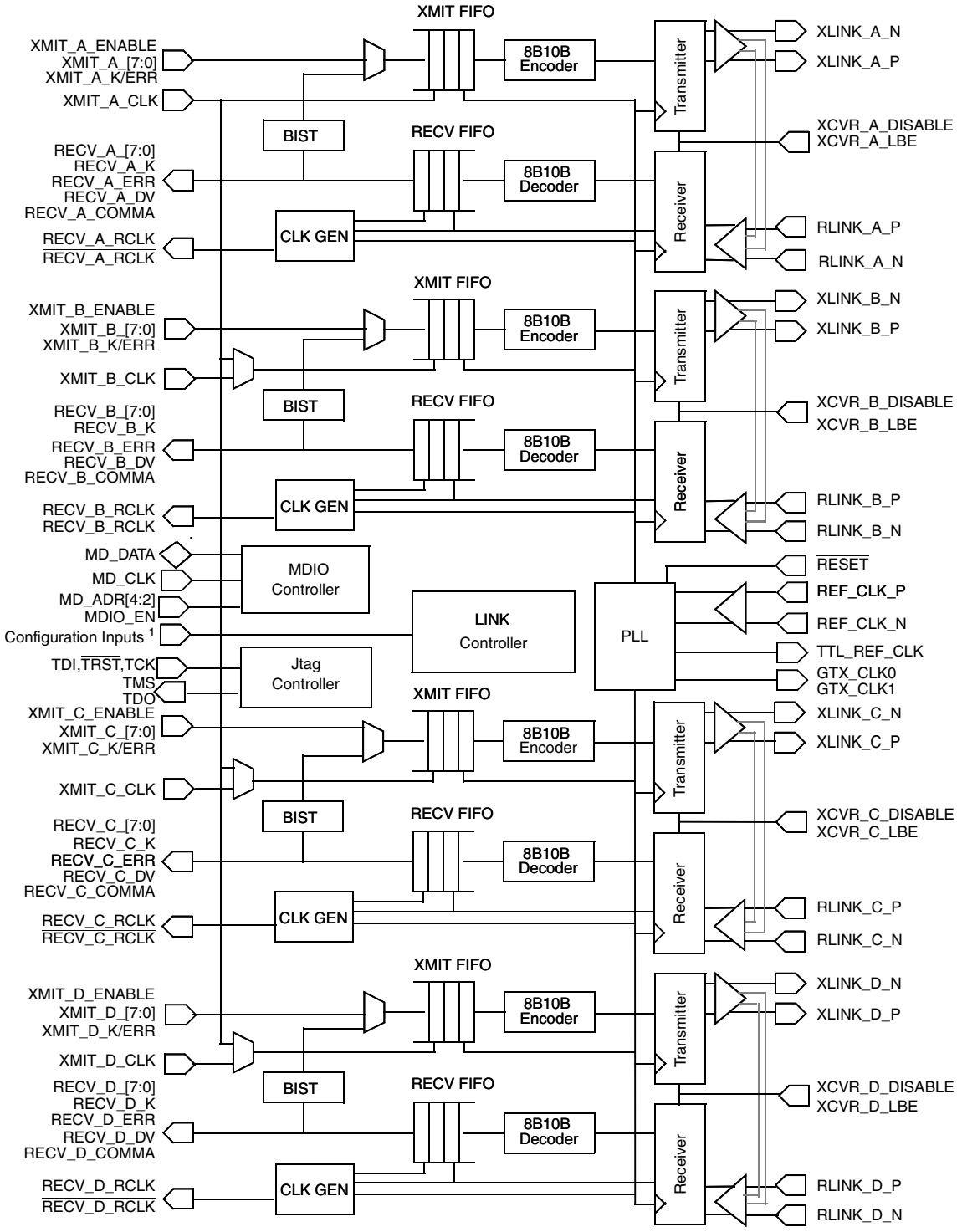


Figure 1-1. MC92603 Simplified Block Diagram



[1] Configuration signal inputs are: RECV_REF_A, COMPAT, REPE, HSE, ADIE, TBIE, BSYNC, LBOE, DROP_SYNC, TST_0, TST_1, WSYNC0, WSYNC1, STNDBY, XMIT_REF_A, MEDIA, RCCE, JPACK, RECV_CLK_CENT, DDR, ENABLE_AN, USE_DIFF_CLK, ENAB_RED, BROADCAST, XCVR_A_RSEL, XCVR_B_RSEL

Figure 1-2. MC92603 Block Diagram

The MC92603 performs the physical coding sublayer (PCS) and the physical medium attachment (PMA) sublayer for 1000BASE-X PHY as defined in clause 36 of the IEEE Std. 802.3-2002 specification [4].

Figure 1-3 shows a typical application for the MC92603 which may be used as a quad 1000BASE-X PHY or in backplane applications. On high density line cards with a large number of Gig-Ethernet ports, it is desirable to use the RGMII interfaces to reduce the number of signal traces on the PCB.

The MC92603 may be used to interface directly to the Gigabit MACs integrated into the MPC PowerQUICC III™ communications processors. They are also interface-compatible to C-Port's C-3 and C-5 network processors available from Freescale.

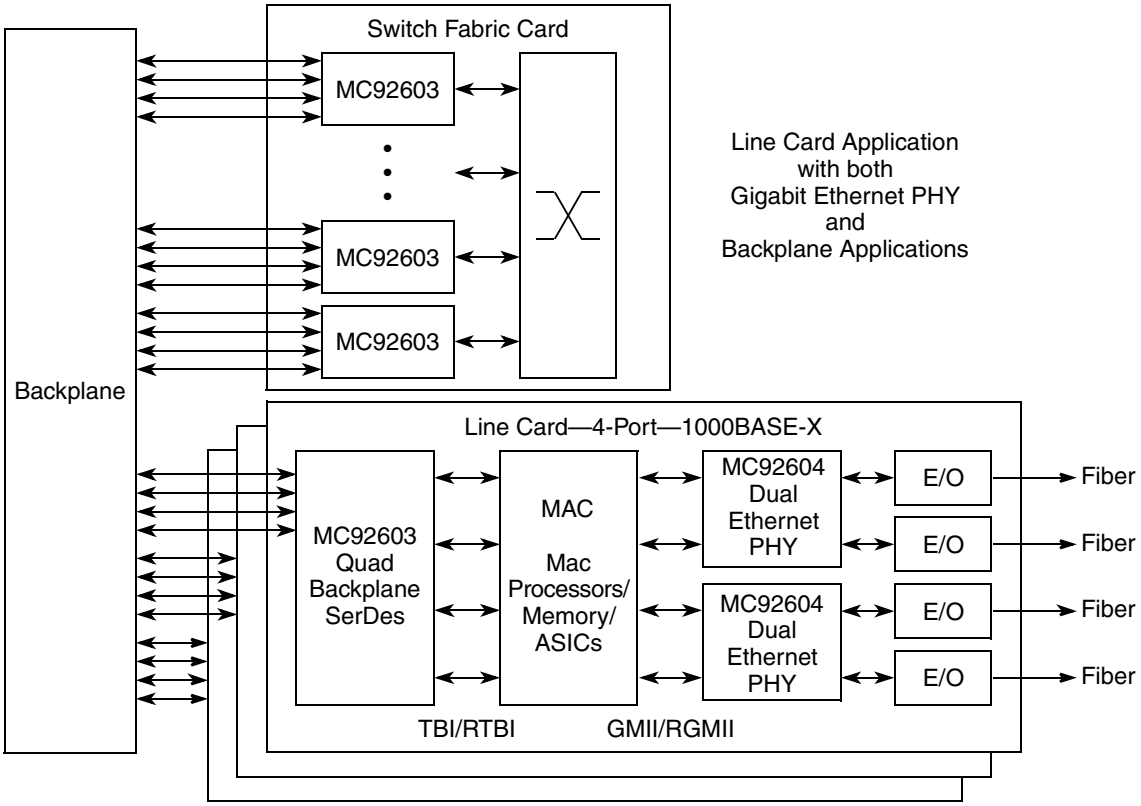


Figure 1-3. PHY and Backplane Applications

1.4 References

The indexed references in this manual are as follows:

[1] *Fibre Channel, Gigabit Communications and I/O for Computer Networks*, Brenner, 1996.

[2] *Byte Oriented DC Balanced 8B/10B Partitioned Block Transmission Code*, U.S. Patent #4,486,739, Dec. 4, 1984.

[3] *IEEE Standard Test Access Port and Boundary-Scan Architecture,* IEEE Std. 1149.1-1990 (includes IEEE Std. 1149.1a-1993), Oct. 1993.

[4] *IEEE Standard Carrier Sense Multiple-Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications,* IEEE Std. 802.3-2002, March 2002.

Chapter 2
Transmitter

This chapter describes the MC92603 transmitter and its interfaces and operation. This chapter consists of the following sections:

The MC92603 is a versatile device that may be used in backplane SerDes or Ethernet PHY applications. It may be configured in multiple data interface and operational modes. The following sections provide a basic functional description of the transmitter, its operational modes, and data interfaces. Each transmitter takes data presented at its source synchronous parallel data input port, creates a transmission code group or character (if not pre-encoded), and serially transmits the code group out of the differential link output pads.

2.1 Transmitter Block Diagram

Figure 2-1 shows a block diagram of the MC92603 transmitter.

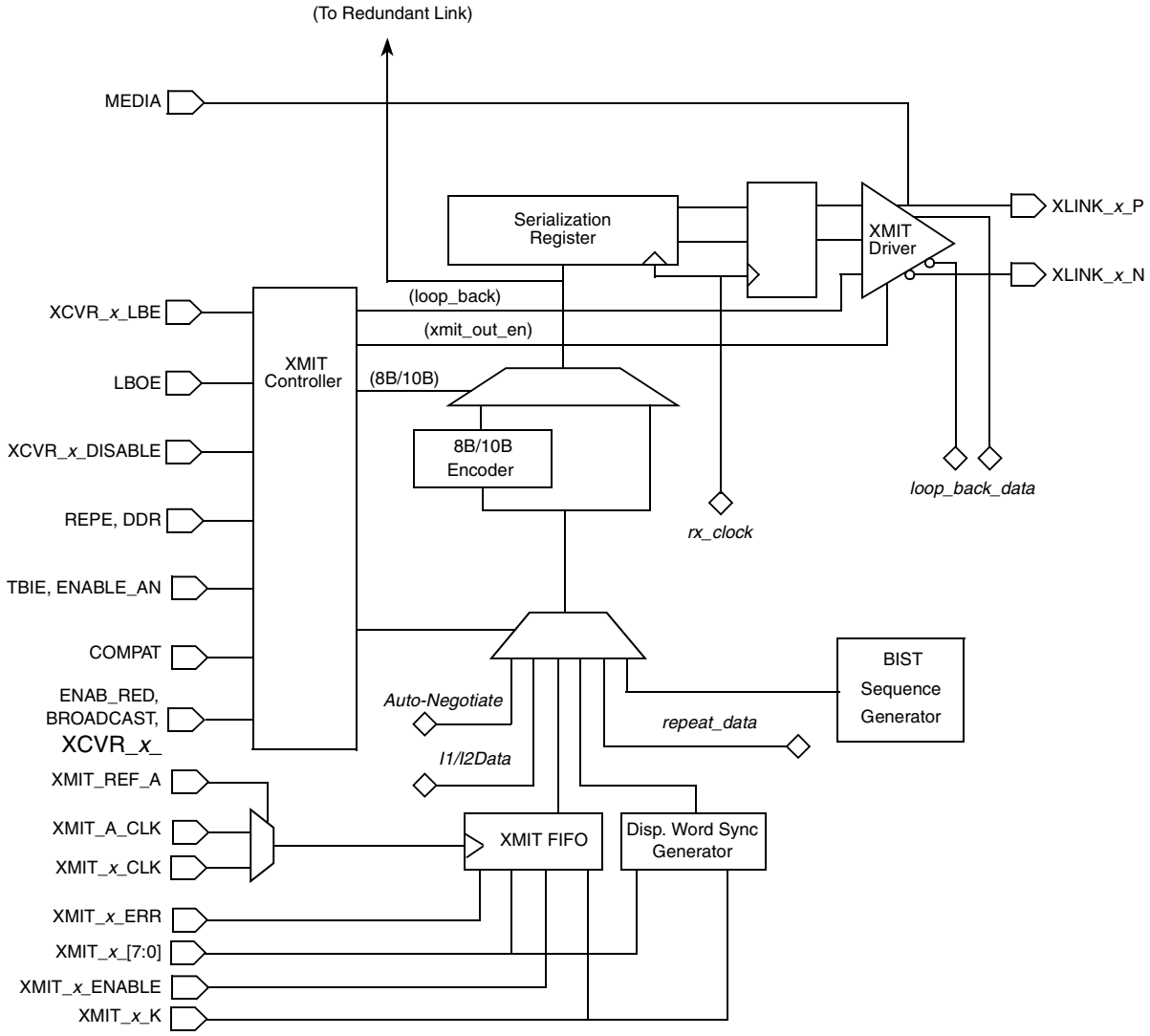


Figure 2-1. MC92603 Transmitter Block Diagram

2.2 Transmitter Interface Signals

This section describes the interface signals of the MC92603 transmitters. Each signal's name, function, direction, and active state is described in Table 2-1. The table's signal names use the letter '*x*' as a place holder for the link identifier letter 'A' through 'D.' Internal signals listed in the table are not available at the external interface of the device but are presented to help illustrate the device's operation.

Table 2-1. MC92603 Transmitter Interface Signals

Signal Name	Description	Function	Direction	Active State
XMIT_*x*_CLK	Channel transmit clock	Clock input for each channel	Input	—
XMIT_*x*_[7:0]	Transmit data byte	8 bits of transmit data	Input	—
XMIT_*x*_K	Transmit control/data bit	If TBIE is high, this input is used by the receiver to enable COMMA realignment. If TBIE and COMPAT are low, this is the 'K' (special character) input.	Input	—
XMIT_*x*_ERR	Transmit control/data bit	If TBIE is high, this is data bit 9. If TBIE and COMPAT are negated low, this is the 'force code error' input. If TBIE is low and COMPAT is high, this input is used as defined for GMII functionality (as defined in IEEE Std. 802.3-2002 specification[4]).	Input	—
XMIT_*x*_ENABLE	Transmit enable data	If TBIE is high, this is data bit 8. If TBIE is low, this input defines transmit data is available on input.	Input	High
XCVR_*x*_LBE	Loopback enable	Activate digital loopback path, such that data transmitted is looped back to corresponding receiver.	Input	High
XCVR_*x*_DISABLE	Transceiver disable	When active this transmitter is disabled.	Input	High
XMIT_REF_A	Transmit interface clock select	Indicates that the transmit interface signals are timed to XMIT_A_CLK instead of individual channel transmit clock.	Input	High
LBOE	Loopback output enable	If LBOE is high, link outputs remain active during digital loopback. If LBOE is low, link outputs are disabled during loopback.	Input	High
REPE	Repeater mode enable	When this input is high, data received on the corresponding receiver is 'repeated' by the transmitter.	Input	High
TBIE	Ten-bit interface enable	Indicates that coded data is on the inputs, bypassing the internal 8B/10B coding.	Input	High
COMPAT	Enable IEEE Std. 802.3-2002 compliance	When enabled, transmitter conforms to IEEE Std. 802.3-2002 [4] GMII or TBI operating modes.	Input	High
DDR	Enable double data rate	When enabled the transmitter accepts 4/5 bits of data on positive edge of XMIT_*x*_CLK and the second 4/5 bits of data on the negative edge.	Input	High
ENABLE_AN	Enable auto-negotiate	Allows the transceiver to perform an auto-negotiate sequence if in GMII mode (COMPAT high, TBIE low)	Input	High
ENAB_RED	Enable redundant link	Enable redundant link operation. Channels A and B available to use with redundant links.	Input	High
BROADCAST	Transmit on both redundant links	Broadcast transmitted data on both of the redundant links for each channel.	Input	High
XCVR_*x*_RSEL	Select redundant link	Transmit data on the secondary (redundant) link	Input	High

Table 2-1. MC92603 Transmitter Interface Signals (continued)

Signal Name	Description	Function	Direction	Active State
TST_1, TST_0	Test mode config inputs	Decoded to define various test modes (see Chapter 6, "Test Features," for details)	Input	—
MEDIA	Media impedance select	Indicates the impedance of the transmission media. Low indicates 50 Ω and high indicates 75 Ω.	Input	—
XLINK_*x*_N/ XLINK_*x*_P	Link serial transmit data	Differential serial transmit data output pads	Output	—
Internal Signals				
rx_clock	High-speed transceiver clock	Internal, differential high speed clock used to transmit and receive link data	Input	—
repeat_data	Received repeat data	Repeater mode, received data to re-transmit	Input	—
loop_back_data	Loopback data	Differential loopback transmit data	Output	—
auto_neg_enable	Auto-negotiation enable	Auto-negotiate is enabled if this signal is high and in GMII mode	Input	High

2.3 Transmitter Interface Configuration

The transmitter may operate in one of eight data interface configurations as shown in Table 2-2. The compatibility configuration pin, COMPAT, establishes operation in either the backplane applications mode or the Ethernet compatible mode. The 10-bit interface enable, TBIE, configuration input, determines if the internal 8B/10B encoder will be used with uncoded input data or bypassed for a pre-encoded (coded) input data. When the DDR configuration pin is enabled, it reduces the interface from an 8-/10-bit single data rate interface to a 4-/5-bit double data rate interface.

The configuration signals, COMPAT and TBIE, also affect the receiver's configuration.

Table 2-2. MC92603 Data Interface Modes

Data Interface Mode	COMPAT	TBIE	DDR
Backplane 8-bit uncoded data	Low	Low	Low
Backplane (4-bit reduced interface) uncoded data	Low	Low	High
Backplane 10-bit coded data	Low	High	Low
Backplane (5-bit reduced interface) coded data	Low	High	High
Ethernet compatible GMII	High	Low	Low
Ethernet compatible RGMII	High	Low	High
Ethernet compatible TBI	High	High	Low
Ethernet compatible RTBI	High	High	High

Transmit data is sampled and stored in the input FIFO on the rising edge (single data rate) of the appropriate transmit clock, if DDR is low, or both edges (double data rate) of the transmit clock if DDR is high. The FIFO accepts data to be transmitted and synchronizes it to the internal clock domain.

The 8B/10B encoder takes an 8-bit data/control from the input register and encodes it into 10-bit transmission characters. The fibre channel 8B/10B coding standard is followed [1,2]. A detailed

explanation of the 8B/10B coding scheme is offered in Appendix B, "8B/10B Coding Scheme." Running disparity is maintained, and the appropriate transmission characters are produced, maintaining DC balance and sufficient transition density to allow reliable data recovery at the receiver. The 8B/10B encoder is bypassed if TBIE is asserted high.

The transmitter data interface operates at high frequency (nominally 125 MHz). In order to ease development of devices that interface with the Gigabit Ethernet transceiver, all transmitter data input interfaces are source-synchronous. The data for each channel has its own dedicated clock input. This allows the clock at the source of the data to be routed with the data ensuring matched delay and timing. However, if per-channel clock sources are not available or deemed unnecessary, all channels may be clocked by a common clock source. This is enabled by asserting XMIT_REF_A high. When XMIT_REF_A is high, the XMIT_A_CLK becomes the interface clock for all active channels.

The configuration settings of the MC92603 affect the legal range of clock frequencies at which it may be operated. Table 5-1 shows legal transmit interface clock frequencies for all modes of operation. All transmit interface clock inputs, XMIT_*x*_CLK, and the PLL reference clock inputs, REF_CLK, must have identical frequencies. The transmit data interface tolerates ±180° of transmit interface clock phase drift relative to the PLL reference clock input.

2.3.1 Transmit Driver Operation

The transmit driver outputs the transmission characters serially across the link. Two bits per internal transceiver clock, *rx_clock*, one each on the rising and falling clock edges, are transmitted differentially from the XLINK_*x*_P/XLINK_*x*_N outputs. The internal *rx_clock* runs at 625 MHz for 1-Gbps (1.25-Gbaud) operation and 312.5 MHz for 500-Mbps (625-Mbaud) operation.

The transmitter driver (high-speed serial link outputs) is a controlled impedance driver. The impedance of the driver is programmable to 50 or 75 Ω through the MEDIA configuration signal. The drive impedance is 50 Ω when MEDIA is low and 75 Ω when high.

2.3.2 Repeater Mode Operation

Although repeater mode is primarily used for factory engineering, it may be used by the application as described in Section 5.5, "Repeater Mode." The repeater enable signal, REPE, should be configured low during a normal transceiver operation.

2.4 Backplane Application Modes (COMPAT = Low)

When the configuration control signal, COMPAT, is low, the MC92603 is in the 'backplane application mode.' In this application mode, the MC92603 transmitters accept either uncoded data, where the input data is encoded internally by an 8B/10B encoder, or coded data, where the input data is pre-encoded and the internal encoder is bypassed.

The interface for the backplane application mode is either 8 or 10 bits wide, or optionally 4 or 5 bits, as shown in Table 2-2.

2.4.1 Transmitting Uncoded Data—8-/4-Bit Modes

The settings for the transmitter control signals when sending uncoded 8-bit or reduced interface 4-bit data is shown in Table 2-3.

When XMIT_*x*_ENABLE is low, an IDLE (K28.5) code group of proper running disparity is generated. The states of the XMIT_*x*_7–XMIT_*x*_0, XMIT_*x*_K, and XMIT_*x*_ERR signals are ignored. This allows the link partner's receiver to maintain alignment when transmission of data is not needed.

Table 2-3. Transmitter Control States for Uncoded Data (TBIE = Low)

XMIT_*x*_ENABLE	XMIT_*x*_ERR	XMIT_*x*_K	Description
Low	Don't care	Don't care	Transmit *IDLE* (K28.5), ignore XMIT_*x*_7–XMIT_*x*_0 data inputs
High	Low	Low	Transmit data present on XMIT_*x*_7–XMIT_*x*_0 data inputs
High	Low	High	Transmit control data present on XMIT_*x*_7–XMIT_*x*_0 data inputs
High	Low	High	Transmit disparity-style word synchronization event if XMIT_*x*_7–0 data inputs = 0xAD. The transmitter inputs will be ignored while sending these 16 code groups.
High	High	Don't care	Create an invalid 10-bit code group to be transmitted

When XMIT_*x*_ENABLE is high, uncoded data is presented in 8-/4-bit bytes to the input register through the XMIT_*x*_7–XMIT_*x*_0 signals. The uncoded data is coded into 10-bit transmission code groups using an on-chip 8B/10B encoder. 8B/10B coding ensures DC balance across the link and sufficient transition density to facilitate reliable data and clock recovery. The XMIT_*x*_7–XMIT_*x*_0 signals are interpreted as normal data when the XMIT_*x*_K signal is low.

The 8B/10B code set includes 12 special control codes. Special control codes may be transmitted by setting the XMIT_*x*_K high as indicated in Table 2-3. There are only 12 valid control code groups; if the data input is other than the 12 defined values, then an illegal 10-bit code group will be generated and transmitted. Invalid combinations of XMIT_*x*_K and XMIT_*x*_7–XMIT_*x*_0 will generate invalid 10-bit code groups.

If XMIT_*x*_ERR is high then the 8B/10B encoder is forced to produce an invalid 10-bit code.

When using the device in a system where word alignment is required, it may be desirable to generate disparity-style word synchronization events. Also, it may be necessary to generate a disparity-style synchronization event for compatibility with legacy transceivers. A disparity-style word synchronization event is generated by setting the transmit data inputs to a 0xAD and asserting XMIT_*x*_K high for the appropriate transmitter(s). The transmitter generates 1 of 2 unique 16-code group IDLE (K28.5) sequences depending on the current running disparity:

I+, I+, I–, I–, I+, I–, I+, I–, I+, I–, I+, I–, I+, I–, I+, I–

or

I–, I–, I+, I+, I–, I+, I–, I+, I–, I+, I–, I+, I–, I+, I–, I+

where I+ stands for K28.5 of positive disparity, and I– stands for K28.5 of negative disparity.

The transmitter inputs, XMIT_*x*_7–XMIT_*x*_0, XMIT_*x*_K, XMIT_*x*_ERR, and XMIT_*x*_ENABLE are ignored for the next 15 byte-times while this 16-code group sequence is transmitted.

Transmitting uncoded data in backplane applications with the reduced interface mode is shown in Table 2-4. The transmitter functional operation is the same as discussed above, except the data is entered on both edges of the transmitter input clock, XMIT_*x*_CLK.

Table 2-4. Transmitter Inputs for Reduced Uncoded Data—Backplane Mode

Data on Rising Edge of XMIT_*x*_CLK	Data on Falling Edge of XMIT_*x*_CLK	MC92603 Signal Name
XMIT_*x*_ENABLE	XMIT_*x*_ENABLE (XOR) XMIT_*x*_ERR	XMIT_*x*_ENABLE
XMIT_*x*_K	Unused	XMIT_*x*_K
Data bits 3–0	Data bits 7–4	XMIT_*x*_3/XMIT_*x*_0

The 8 bits of uncoded data are entered with the least significant nibble on the rising clock and the most significant nibble on the falling clock edge.

NOTE

When operating with the reduced data interface the MC92603 input pins, XMIT_*x*_7–XMIT_*x*_4, are unused and should be terminated low.

2.4.2 Transmitting Coded Data—10-/5-Bit Modes

This operating mode is specified when the TBIE input is high. The state of COMPAT input does not affect the transmitter's operation.

In this mode, 10-bit coded data may be transmitted, bypassing the internal 8B/10B encoder. The 10 bits of data to transmit are presented on the XMIT_*x*_7–XMIT_*x*_0 inputs along with bits 9 and 8 on the XMIT_*x*_ERR and XMIT_*x*_ENABLE inputs, respectively. The 10-bit coded data is transmitted as shown in Table 2-5.

Table 2-5. Transmitter Input States for Coded Data (TBIE = High)

XMIT_*x*_K	XMIT_*x*_ERR	XMIT_*x*_ENABLE	XMIT_*x*_7–XMIT_*x*_0	Description
Used by receiver	Data bit 9	Data bit 8	Data bits 7–0	Data bits 9–0

The XMIT_*x*_K signal is ignored by the transmitter in the backplane 10-/5-bit modes, but, it is used by the receiver.

When using the MC92603 in the backplane applications (COMPAT = low), it is not necessary to use the 8B/10B code set. However, special care must be taken. The data must exhibit the same properties as 8B/10B coded data. DC balance must be maintained and there must be sufficient transition density to ensure reliable clock and data recovery at the receiver. If running in the Ethernet TBI or RTBI mode, the data will be 8B/10B data.

NOTE

If the code used is not 8B/10B, then it must support the K28.5 IDLE code (this only applies to backplane mode; Ethernet-TBI mode is assumed to use 8B/10B). The code must be such to guarantee that no two codes, when concatenated, produce the 8-bit COMMA pattern as defined above.

The receivers require that COMMA code groups (K28.1, K28.5, or K28.7) be transmitted for byte synchronization. The 8-bit pattern (‘00111110xx’ or ‘11000001xx,’ ordered from bits 0–7) is used for alignment and link-to-link synchronization when operating in any of the byte or word synchronization modes. The pattern of code groups and data required to achieve word synchronization (available only in backplane application mode, COMPAT = low) depends on the configuration of the receiver. The appropriate sequence must be applied through the 10-/5-bit interface.

Transmitting coded data with the reduced interface mode is shown in Table 2-6. The transmitter functional operation is the same as discussed above, except the data is entered on both edges of the transmitter input clock, XMIT_*x*_CLK.

Table 2-6. Transmitter Inputs for RTBI Operating Mode

Data on Rising Edge of XMIT_*x*_CLK	Data on Falling Edge of XMIT_*x*_CLK	MC92603 Signal Name
Data bit 4	Data bit 9	XMIT_*x*_ENABLE
Data bits 3–0	Data bits 8–5	XMIT_*x*_3/XMIT_*x*_0

The 10 bits of uncoded data are entered with the least significant 5 bits on the rising clock and the most significant bits on the falling clock edge.

2.5 Ethernet Compliant Applications Modes (COMPAT = High)

The MC92603 Gigabit Ethernet transceiver was designed with the intent to meet the requirements of **IEEE Std 802.3-2002 [4]** for 1000BASE-X PHYs.

When the configuration control signal, COMPAT, is high, the MC92603 is in the 'Ethernet compliant application mode.' In this application mode, the MC92603 transmitters accept either uncoded data (GMII or RGMII interface), where the input data is encoded internally by an 8B/10B encoder, or coded data (TBI or RTBI interface), where the input data is pre-encoded and the internal encoder is bypassed. See Table 2-2 for these interface modes. Table 2-7 defines the ordered_sets that are associated with the Gigabit Ethernet protocol.

Table 2-7. Gigabit Ethernet Defined Ordered Sets

Code	Ordered_Set	Number of Code-Groups	Encoding
/**C**/	Configuration	—	Alternating /C1/ and /C2/
/C1/	Configuration 1	4	/K28.5/D21.5/Config_Reg
/C2/	Configuration 2	4	/K28.5/D2.2/Config_Reg
/**I**/	IDLE	—	Correcting /I1/, Preserving /I2/
/I1/	IDLE1	2	/K28.5/D5.6/
/I2/	IDLE2	2	/K28.5/D16.2/
Encapsulation			
/R/	Carrier_Extend	1	/K23.7/
/S/	Start_of_Packet	1	/K27.7/
/T/	End_of_Packet	1	/K29.7/
/V/	Error_Propagation	1	/K30.7/

2.5.1 Transmitting Uncoded Data—GMII or RGMII Modes

The following sections discuss the operating process for uncoded data (GMII or RGMII interface) transmissions.

2.5.1.1 Auto-Negotiation Process

Operating in the Ethernet compatibility mode, the MC92603 implements the auto-negotiation function at the PCS sublayer for 1000BASE-X as defined in Clause 37 of IEEE Std 802.3-2002 specification [4].

The transmitter enters auto-negotiate mode (if auto-negotiate is enabled) when one of five events occur.

- The part is reset
- The part is requested to restart the auto-negotiation process through the MDIO interface
- The part is reconfigured through the MDIO interface
- The associated receiver loses byte synchronization
- The associated receiver detects an auto-negotiate sequence initiated by its link partner

When an auto-negotiate sequence is started, the transmitter initially sends at least 10 milliseconds of /C1/C2/ sequences with all zeros as the Configuration Register contents. This forces the remote device to also enter auto-negotiate mode.

The contents of the configuration register are continuously sent until the associated receiver detects the compatible configuration being sent from the link partner. The MC92603 is configured as full-duplex 1-Gigabit; therefore, the configuration is as shown in Figure 2-2. For register details, see Section 4.2.4, "MDIO RA 4—Auto-Negotiation Advertisement Register."

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	Next Page[1]	Ack[2]	RF2[3]	RF1[3]	Reserved			PS2[4]	PS1[4]	HD[5]	FD[6]	Reserved				
Value	0	1/0	1/0	1/0	0	0	0	0	0	0	1	0	0	0	0	0

[1] Next Page—MC92603 does not support multiple pages of configuration registers.

[2] Ack—Asserted when the receiver detects a valid configuration from the other transmitter.

[3] RF1 and RF2— 'Remote faults' as detected by the receiver.

[4] PS1 and PS2—Pause control bits that reflect the values of MDIO register 4's bits 12 and 13, respectively. This register may be modified via the MDIO interface.

[5] HD—MC92603 does not support half-duplex mode.

[6] FD—MC92603 always runs in full-duplex mode.

Figure 2-2. Configuration Register

The 'Ack' bit is asserted when three consecutive matching configuration register values are received. The auto-negotiate state is complete when three consecutive matching configuration register values are received with the 'Ack' bit set. The transmitter continues sending auto-negotiate sequences once the auto-negotiate sequence is complete for at least 10 ms.

NOTE

See the state diagram in Figure 37-6 of the IEEE Std. 802.3-2002 specification [4] for a complete description.

2.5.1.2 Ethernet Data Transmission Process

Transmitter operation is controlled by the two input control signals XMIT_*x*_ENABLE and XMIT_*x*_ERR. See Table 3-9 for the complete GMII interface to the MC92603.

When both XMIT_*x*_ENABLE and XMIT_*x*_ERR inputs are low, the transmitter broadcasts IDLE Ordered_sets. Whenever a new series of IDLE Ordered_sets are started, the first IDLE Ordered_set may be an I1 Ordered_set to correct the running disparity, all subsequent IDLE Ordered sets will be I2s. The transmitter must be aware of even/oddness. K28.5 code groups are transmitted as the 'even' code group and either D5.6 or D16.2 as the 'odd' code group. This even/odd flag is set at initialization and must be maintained since other events will depend on this even/oddness.

When XMIT_*x*_ENABLE is raised, the data on the XMIT_*x*_7 through XMIT_*x*_0 inputs is assumed to be the first byte of an 8-byte preamble. The preamble usually consists of 7 consecutive 0x55 code groups followed by a 0xD5 code group. The transmitter replaces the first 0x55 code group in the preamble with a

/S/ Ordered_set to indicate Start_of_Frame. The MC92603 will support shorter preambles. The minimum preamble size is a single 0x55 code group followed by a 0xD5 code group.

If XMIT_*x*_ERR is also raised when XMIT_*x*_ENABLE is raised, then a false carrier is declared, and a void code groups (/V/) is transmitted.

If XMIT_*x*_ERR is raised after XMIT_*x*_ENABLE has been raised and while data is being transferred, this is a request to transmit an error propagation Ordered_set (/V/) for as many code groups as long as XMIT_*x*_ERR remains high.

When a normal End_of_Packet is detected (XMIT_*x*_ENABLE transitions to low and XMIT_*x*_ERR remains low), a single End_of_Packet ordered_set (/T/) is transmitted followed by at least one Carrier_Extend (/R/) ordered_set. A second Carrier_Extend will be inserted (if necessary) to complete an even/odd pair. This is then followed by IDLE ordered_sets to indicate the inter-packet gap. The first /I/ may be either an /I1/ or /I2/, depending on running disparity.

If XMIT_*x*_ERR transitions to high as XMIT_*x*_ENABLE transitions to low, this is defined as a ‘carrier extension.’ The ‘carrier extension’ state is a half-duplex feature and is not supported in the MC92603.

XMIT_*x*_ERR will be ignored while XMIT_*x*_ENABLE is low.

Transmitting in the Ethernet-compatability mode with the reduced (RGMII) interface is shown in Table 2-8. The transmitter functional operation is the same as discussed above, except the data is entered on both edges of the transmitter input clock, XMIT_*x*_CLK.

Table 2-8. Transmitter Inputs for RGMII Operating Mode

Data on Rising Edge of XMIT_*x*_CLK	Data on Falling Edge of XMIT_*x*_CLK	MC92603 Signal Name
GMII_TX_EN	GMII_TX_EN (XOR) GMII_TX_ER	XMIT_*x*_ENABLE
Data bits 3–0	Data bits 7–4	XMIT_*x*_3/XMIT_*x*_0

The 8 bits of uncoded data are entered with the least significant 4 bits on the rising clock and the most significant bits on the falling clock edge.

2.5.2 Transmitting Coded Data—TBI or RTBI Modes

The PMA sublayer of the 1000BASE-X specification does not require any functional differences in the transmitter from that used in the backplane application mode. Therefore, when operating in a mode specified when the TBIE input is high, the state of the COMPAT input does not affect the transmitter’s operation. See Section 2.4.2, “Transmitting Coded Data—10-/5-Bit Modes.”

2.6 Transmitter Redundant Link Operation

The MC92603 is configured as a dual channel SerDes, with redundant link input and outputs, if the enable redundancy signal, ENAB_RED, is asserted high. Only the data interface to channels A and B will accept data to be transmitted. This data will be transmitted over the appropriate link as specified by the BROADCAST and XCVR_x_RSEL inputs as shown in Table 2-9.

NOTE

When operating in the redundancy mode, the transmitter channels C and D input signals (XMIT_C_--- and XMIT_D_---), should be terminated low.

XCVR_A_RSEL, and XCVR_B_RSEL selects the primary or secondary link I/Os for channels A and B, respectively. The BROADCAST control signal enables both channel A and B link outputs to transmit data at their data interface, while enabling the receiver links to receive serial data defined by the XCVR_x_RSEL control signal. See Section 3.3.6, "Receiver Redundant Link Operation," for more on receiver redundancy.

Table 2-9. Transmit Channel A Redundant Link Operation

ENAB_RED	BROADCAST	XCVR_A_RSEL	Action
0	Don't care	Don't care	Data transmitted over XLINK_A_P/XLINK_A_N.
1	0	0	Data transmitted over XLINK_A_P/XLINK_A_N.
1	0	1	Data transmitted over XLINK_C_P/XLINK_C_N.
1	1	Don't care	Data transmitted over XLINK_A_P/XLINK_A_N and XLINK_C_P / XLINK_C_N.

Table 2-10. Transmit Channel B Redundant Link Operation

ENAB_RED	BROADCAST	XCVR_B_RSEL	Action
0	Don't care	Don't care	Data transmitted over XLINK_B_P/XLINK_B_N.
1	0	0	Data transmitted over XLINK_B_P/XLINK_B_N.
1	0	1	Data transmitted over XLINK_D_P/XLINK_D_N.
1	1	Don't care	Data transmitted over XLINK_B_P/XLINK_B_N and XLINK_D_P/XLINK_D_N.

Chapter 3
Receiver

This chapter describes the MC92603 receiver, its interfaces, and operation. This chapter consists of the following sections:

3.1 Receiver Block Diagram

Figure 3-1 shows the MC92603 receiver's block diagram.

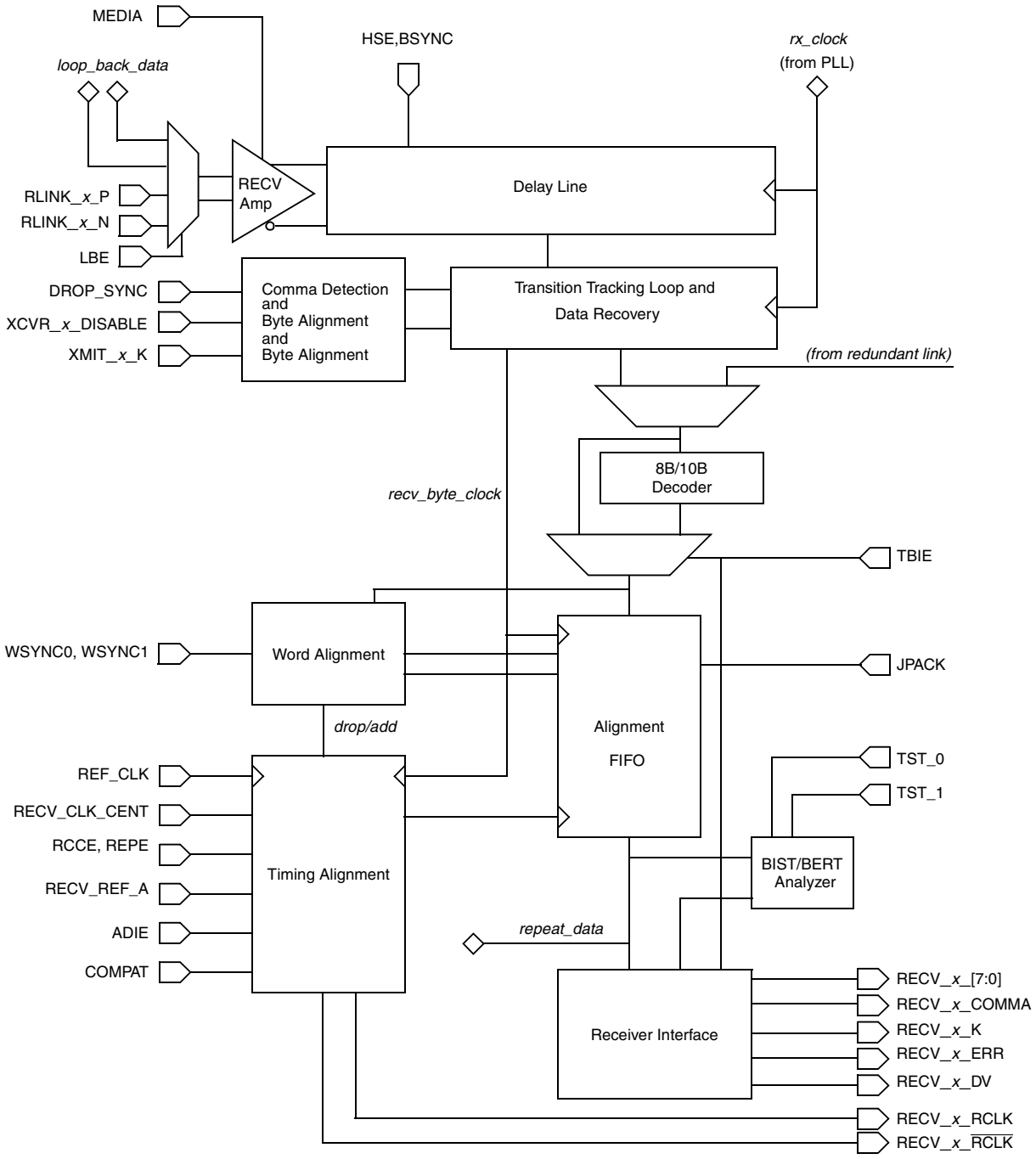


Figure 3-1. MC92603 Receiver Block Diagram

3.2 Receiver Interface Signals

This section describes the interface signals of the MC92603 receiver. Each signal's name, function, direction, and active state is described in Table 3-1. The table's signal names use the letter '*x*' as a place holder for the link identifier letter 'A' through 'D.' Internal signals listed in the table are not available at the external interface of the device, but are presented to help illustrate the device's operation.

Table 3-1. MC92603 Receiver Interface Signals

Signal Name	Description	Function	Direction	Active State
RECV_*x*_[7:0]	Received byte	Receive data bits 7 through 0	Output	—
RECV_*x*_DV	Data valid indicator	If TBIE is high, this is the receive data, bit 8. If TBIE is low, this is data valid indicator.	Output	—
RECV_*x*_K	Special data indicator	If TBIE is high, this indicates that receiver has detected an error. The type of error is indicated in the data byte (RECV_*x*_7–RECV_*x*_0). If TBIE is low, this indicates whether the 8-bit receive data is a 'special' code group.	Output	—
RECV_*x*_COMMA	COMMA indicator	This is the COMMA DETECT indicator.		
RECV_*x*_ERR	Receiver error	If TBIE is high, this is receive data, bit 9. If TBIE is low, see Table 3-10 and Table 3-15.	Output	—
RECV_*x*_RCLK	Receiver clock	Internally generated clock synchronized with receiver data. If TBIE is high, then this clock frequency is half of the data frequency.	Output	—
RECV_*x*_RCLK_B	Receiver clock complement	If TBIE is high, this is the complement of RECV_*x*_RCLK. If TBIE is low, this signal is low.	Output	—
XCVR_*x*_DISABLE	Transceiver disable	When active receiver is disabled	Input	High
XMIT_*x*_K	Transmitter/receiver input	If TBIE is high, XMIT_*x*_K enables automatic realignment on COMMA code groups. If XMIT_*x*_K is low, initial alignment on COMMAs occurs but subsequent realignments are disabled. If TBIE is low, this signal is used by the transmitter logic and ignored by the receiver logic.	Input	—
JPACK	Enable Jumbo frames	When high, this signal increases the depth of the receive FIFO allowing longer packets of data between bytes that may be repeated or dropped to prevent overruns or underruns. Only needed if RCCE is low (reference clock mode).	Input	High
RECV_REF_A	Receiver A clock enable	If RECV_REF_A and RCCE are high, then data will be synchronized to Channel A's recovered clock.	Input	High
WSYNC1 & WSYNC0	Word synchronization modes	If either input is high, then all enabled receivers are being used in unison to receive synchronized data.	Input	High
BSYNC	Byte alignment mode	Indicates that byte alignment is required. If it is low, no byte alignment is done.	Input	—

Table 3-1. MC92603 Receiver Interface Signals (continued)

Signal Name	Description	Function	Direction	Active State
COMPAT	IEEE Std. 802.3-2002 compatibility mode enable	Indicates that the receiver is in a IEEE Std. 802.3-2002 compliant mode. If code group addition/deletion is required to maintain alignment, then special rules are followed that non-intrusive to the IEEE Std. 802.3-2002 packet streams. See Section 3.7.2, "Rate Adaption of Ethernet Packet Data Streams," for more information.	Input	High
XCVR_*x*_LBE	Enable loopback	Indicates that data into the receiver is to be taken from the corresponding transmitter.	Input	High
DROP_SYNC	Drop synchronization	DROP_SYNC may be used with XCVR_*x*_DISABLE to force a receiver to resync, but it does not affect the transmitter operation.	Input	High
RCCE	Recovered clock enable	Indicates that the output data is synchronized to a recovered clock.	Input	High
ADIE	Add/delete idle enable	Indicates that the receiver is free to add/delete code groups to/from the output data stream to maintain alignment. See Section 3.7.2, "Rate Adaption of Ethernet Packet Data Streams," for more information. This input is ignored if RCCE is high.	Input	High
TBIE	Ten-bit interface enable	Indicates that the receiver interface is in a 10-bit mode, and that the 8B/10B decoder is bypassed.	Input	High
HSE	Half-speed enable	Indicates that the link and data interfaces are to be operated at half-speed.	Input	High
REPE	Repeater mode enable	Causes data received to be transmitted over the corresponding transmit channel. See Section 5.5, "Repeater Mode," for details.	Input	High
ENAB_RED	Enable redundant mode	Enable redundant link operation.	Input	High
XCVR_*x*_RSEL	Select redundant channel	Receive data from secondary (redundant) channel.	Input	High
MEDIA	Media impedance select	Indicates the impedance of the transmission media. When the MEDIA signal is negated low, it indicates 50 Ω and when asserted high, it indicates 75 Ω.	Input	—
RECV_CLK_CENT	Center recovered clock	Indicates that the recovered clocks (RECV_*x*_RCLK and RECV_*x*_RCLK_B) will be centered relative to the receive data and status outputs.	Input	High
TST_0/TST_1	Test mode	Indicates the operating/test mode of the device.	Input	—
REF_CLK_P/N	PLL reference clock	PLL reference clock input. The signal also provides reference frequency for the receiver interface when recovered clock mode is disabled (RCCE is low).	Input	—
RLINK_*x*_N/ RLINK_*x*_P	Link serial receive data	Differential serial receive data input pads	Input	—
Internal Signals				
rx_clock	High-speed clock	Internal, differential high speed clock, used to transmit and receive link data.	Input	—
loop_back_data	Loopback data	Differential loopback receive data	Input	—
repeat_data	Repeater data	Data received that is looped to the transmitter if in repeater mode (REPE is asserted high). Test feature only.	Output	—

3.3 Functional Description

The MC92603 receiver receives differential data in one of two operating ranges. It may be operated in full rate range with a maximum data rate of 1.0 Gbps (1.25 Gigabaud) or at half-rate at 500 Mbps (0.625 Gigabaud). The operating range is determined by the state of the HSE input and the frequency of the reference clock, see Table 5-1.

Transmitted data is recovered using an oversampled transition tracking method. The received serial data is accumulated into 10-bit characters. The 10-bit characters are forwarded to the 8B/10B decoder where the original data is obtained. Alternately, the decoder can be bypassed, and the 10-bit character is forwarded to the receiver interface in the 10-bit interface (TBI) mode.

The receiver provides for byte (character) alignment. Alignment assures that the byte, presented at the input of the transmitter is preserved when it is presented by the receiver. Optionally, alignment may be disabled if in the backplane 10- or 5-bit mode.

The code group alignment is obtained by aligning to COMMA (K28.1, K28.5, or K28.7) code groups. Alignment is achieved when four COMMA code groups with the same alignment, are detected.

NOTE

The COMMA code group (K28.7) should be used carefully since the combination of this code group with some adjoining code groups will yield false COMMA alignment.

The receiver also provides for word synchronization (this feature is available only in ‘backplane’ operating modes). In this mode, all of the receivers are being used cooperatively to receive 32-bit (40-bit in TBI mode) words. Word synchronization ensures that the receivers present the 4 bytes of a word simultaneously.

At the receiver interface is where the received bytes and status codes are obtained. The receiver interface has several modes of operation and timing that allow it to be used in a variety of applications. The following sections provide a detailed description of the receiver and its modes of operation.

3.3.1 Input Amplifier

The input amplifiers connect directly to the link input pads RLINK_*x*_P and RLINK_*x*_N. It is a differential amplifier with an integrated analog multiplexer for loopback testing. Link termination resistors are integrated with the amplifier. The termination resistance is either 100 or 150 Ω differential depending on the state of the MEDIA configuration input pin. Termination resistance is 100 Ω (differential) when the MEDIA is low and 150 Ω (differential) when the MEDIA is high.

The input amplifier facilitates a loopback path for production and in-system testing. When the MC92603 is in loopback mode (loopback enable, LBE, is high), the input amplifier selects the loopback differential input signals and ignores the state on the RLINK_*x*_P and RLINK_*x*_N signals. This allows in-system loopback BIST independent of the current input state. See Chapter 6, “Test Features,” for complete information on test modes.

3.3.2 Transition Tracking Loop and Data Recovery

The received differential data from the input amplifier is sent to the transition tracking loop for data recovery. The MC92603 uses an oversampled transition tracking loop method for data recovery.

The differentially received data is sampled and processed digitally to provide for low-bit error rate (better than 10^{-12}).

The transition tracking loop is tolerant of frequency offset between the transmitter and receiver. The MC92603 reliably operates with $\pm$250 ppm of frequency offset. The transition tracking loop method is different than the typical PLL clock recovery method. Its receiver compensates for overrun and underrun due to frequency offset. The receiver does this by modulating the duty-cycle and period of the received byte clock so that it matches the frequency of the received data (see Section 3.6.1, "Recovered Clock Timing Mode (RCCE = High)," for more information).

Recovered data is accumulated into 10-bit characters. If a byte alignment mode is enabled by asserting BSYNC high, the characters are aligned to their original 10-bit boundaries.

3.3.3 8B/10B Decoder

The 8B/10B decoder takes the 10-bit character from the transition tracking loop and decodes it according to the 8B/10B coding standard [1,2]. The decoder does two types of error checking. First, it checks that all characters are legal members of the 8B/10B coding space. The decoder also checks for running disparity errors. A disparity error is generated if the running disparity exceeds the limits set in the 8B/10B coding standard.

An illegal character or disparity error asserts the RECV_*x*_ERR signal high, coincident with the received data for a 1-byte output period. The 'code error' or 'disparity error' is being reported as described in Table 3-10 and Table 3-15. It is difficult to determine the exact byte that causes a disparity error, so the error should not be associated with a particular received byte. Rather, it is a general indicator of the improper operation of the link. Use of the disparity error is provided so the system can monitor link reliability.

The 8B/10B decoder is bypassed when operating in 10-bit interface mode (TBIE asserted high).

3.3.4 Half-Speed Mode

Half-speed mode, enabled when HSE is asserted high, operates the receiver in its lower speed range. In half-speed mode, the link speed is 500 Mbps (625 Mbaud). The receiver interface operates at half-speed as well, in pace with the received data.

3.3.5 Repeater Mode

Although repeater mode is primarily used for factory engineering, it may be used by the application, as described in Section 5.5, "Repeater Mode."

3.3.6 Receiver Redundant Link Operation

The MC92603 is configured as a dual channel SerDes with redundant links if the enable redundancy signal, ENAB_RED, is high. Only channels A and B received data interfaces are active in this mode. This data will be received from the appropriate link, as specified by the XCVR_A_RSEL and XCVR_B_RSEL inputs shown in Table 3-2 and Table 3-3.

ENAB_RED is considered a basic configuration input, meaning that it is assumed ENAB_RED will not change states during operation. If the state of ENAB_RED is changed, then the part must be reset.

XCVR_A_RSEL and XCVR_B_RSEL inputs may be changed at any time. However, when the state of this input is changed, the channel will lose synchronization and require COMMAs in the data stream to regain alignment.

Table 3-2. Receiver Channel A Redundant Link Operation

ENAB_RED	XCVR_A_RSEL	Action
0	Don't care	Channel A data is received from RLINK_A_P / RLINK_A_N.
1	0	Channel A data is received from RLINK_A_P / RLINK_A_N.
1	1	Channel A data is received from RLINK_C_P / RLINK_C_N.

Table 3-3. Receiver Channel B Redundant Link Operation

ENAB_RED	XCVR_B_RSEL	Action
0	Don't care	Channel B data is received from RLINK_B_P / RLINK_B_N.
1	0	Channel B data is received from RLINK_B_P / RLINK_B_N.
1	1	Channel B data is received from RLINK_D_P / RLINK_D_N.

3.4 Receiver Interface Configuration

The receiver interface facilitates transfer of received data to the system. Along with the data, information is also provided on the status of the link. Table 3-1 describes the signals involved in the receiver configuration and operation. The receiver interface, through which received data is obtained, may be operated in five operating modes as described in Table 3-4.

Table 3-4. MC92603 Receiver Operating Modes (Common Features/Characteristics)

Operating Mode	BSYNC	COMPAT	TBIE
Backplane 10- or 5-bit coded data modes—non-aligned	Low	Low	High
Backplane 10- or 5-bit coded data modes—aligned	High	Low	High
Backplane 8- or 4-bit byte modes	High	Low	Low
GMII or RGMII compatible mode	High	High	Low
TBI or RTBI compatible mode	High	High	High

The interface may be operated in the byte mode (8 bits) or in the 10-bit interface, TBI, mode. Received data is a byte (8 bits) of uncoded data, when in the backplane byte or GMII modes. In these modes, the

internal 8B/10B decoder was used to decode data from the received 10-bit character. Byte interface mode is enabled by negating TBIE low.

Received data is 10-bits of pre-coded data when in the 10-bit interface, TBI, mode. The internal 8B/10B decoder is not used, and it is assumed that decoding is done externally. The 10-bit interface mode is enabled by asserting TBIE high.

The received data is presented on the interface RECV_*x*_7 through RECV_*x*_0 signals when operating in the GMII or 8-bit backplane modes. In the 10-bit backplane or TBI modes, RECV_*x*_ERR, RECV_*x*_DV become bits 9 and 8, respectively.

In the reduced interface operational modes, the receiver signals RECV_*x*_7 through RECV_*x*_4 are not used and the 5th and 9th data bits are output on the RECV_*x*_DV signal. With the reduced interface, data in the alignment FIFO is presented at the receiver interface as double data rate (DDR), on the rising and falling edge of the appropriate receiver clock, RECV_*x*_RCLK.

The receiver status and error reporting is coded onto the RECV_*x*_ERR, RECV_*x*_DV, RECV_*x*_COMMA, and RECV_*x*_K signals.

All of the digital outputs of the device are internally “source terminated” and therefore do not require exernal series resistors on the pcb. This applies to all received data, status, and clock outputs on the MC92603.

3.5 Data Alignment Configurations

The receiver supports two modes of byte alignment as defined by the BSYNC signal. Table 3-5 shows the settings to activate each mode.

Table 3-5. Byte Synchronization Modes

Byte Alignment Mode	BSYNC
Byte Aligned	High
Non-Aligned	Low

NOTE

Do not use non-aligned mode (BSYNC = low) in 8-bit modes. The non-aligned mode is only valid if TBIE is high.

3.5.1 Non-Aligned Mode (BSYNC = Low)

In non-aligned mode no attempt is made to align the incoming data stream. The bits are simply accumulated into 10-bit code groups and forwarded. This mode should be used only with backplane 10- or 5-bit data mode (TBIE = high, COMPAT = low), and with word synchronization disabled (WSYNC1 = low and WSYNC0 = low).

3.5.2 Byte-Aligned Mode (BSYNC = High)

The remaining 4 receiver operating modes, shown in Table 3-4 align the incoming serial data into 10-bit code groups. At power up, the receiver starts an alignment procedure, searching for the 8-bit pattern

defined by the 8B/10B COMMA codes. Synchronization logic checks for the distinct sequence, ‘00111110xx’ and ‘11000001xx’ (ordered bit 0–7), characteristic of the three valid COMMA code group patterns. The search is done on the 10-bit data in the receiver, and is, therefore, independent of the state of TBIE or COMPAT. Alignment requires a minimum of four, error-free, received COMMA code groups to ensure proper alignment and lock. Non-COMMA code groups may be interspersed with the COMMA code groups. The disparity of the COMMA code groups is not important to alignment and can be positive, negative, or any combination. The receiver begins to forward received code groups once locked on an alignment.

If in the GMII or RGMII mode, alignment is acquired per the PCS state diagram as shown in Figure 36-9 of the IEEE Std. 802.3 2002 specification [4].

Alignment remains locked until any one of three events occur that indicate loss of alignment:

- Alignment is lost when a misaligned COMMA sequence is detected. The MC92603 can be configured to automatically realign to a new COMMA sequence. This mode is always enabled when in backplane byte mode or GMII mode (TBIE low) or when both XMIT_*x*_K and TBIE are high. If automatic realignment is allowed then alignment is lost (and immediately regained) when a misaligned COMMA sequence is detected. A misaligned COMMA sequence is defined as four COMMA code groups with a new alignment other than the current alignment. Non-COMMA code groups can be dispersed between the four misaligned COMMAs; however, a properly-aligned COMMA code group or a COMMA code group with yet another alignment breaks the sequence. When alignment is lost due to misaligned COMMAs, the receiver is automatically aligned to the new COMMA sequence and data continues without interruption. Also, if realignment is allowed by the state of XMIT_*x*_K when in TBI mode, the FIFOs are automatically realigned to keep all IDLE code group output relative to RECV_*x*_RCLK_B (see Section 3.7.1.2, “TBI Operation”). If word synchronization is enabled, any byte realignment will cause loss of word synchronization (see Section 3.5.3.1, “Word Synchronization Method”).
- If the 8B/10B encoder is enabled (TBIE = low), alignment is also lost when the number of received code groups with 8B/10B coding errors outnumbers the non-errored code groups by four. Credit for non-errored code groups in excess of errored code groups is limited to four, such that alignment is lost after four consecutive errored code groups. The receiver restarts its alignment procedure and halts data flow until alignment is achieved.
- Finally, the user may force loss of alignment by asserting XCVR_*x*_DISABLE (high). Each receiver may thus be forced to restart its alignment procedure. Data flow will halt until alignment is achieved. Normally, XCVR_*x*_DISABLE will also disable the transmitter. If this is not desired, raising DROP_SYNC concurrent with (or prior to) XCVR_*x*_DISABLE will force the receiver to re-align and have no effect on the corresponding transmitter.

NOTE

Since XCVR_*x*_DISABLE and DROP_SYNC are not synchronous to the internal clock domain DROP_SYNC should be raised prior to XCVR_*x*_DISABLE is raised and remain high until after XCVR_*x*_DISABLE is negated low.

When establishing byte alignment, or when data flow is halted due to misalignment, the ‘Not Byte Sync’ error is reported as described in Section 3.7.3, “Error Handling.”

3.5.3 Word Synchronization

When the MC92603 is configured in either of the ‘aligned backplane’ modes (BSYNC high and COMPAT low), the four receivers can be used cooperatively to receive 32-bit (40-bit if TBIE is high) aligned word transfers. Word alignment is enabled by asserting the word synchronization enable inputs, WSYNC1 or WSYNC0, high.

3.5.3.1 Word Synchronization Method

The word synchronization aligns code groups in the receiver’s alignment FIFO. Synchronization is accomplished by lining up word synchronization events detected by each of the receivers, such that all are coincident at the same output stage of their FIFO.

There are three word synchronization events as defined in Table 3-6.

Table 3-6. Word Synchronization Events

Word Synchronization Event	WSYNC1	WSYNC0
No word synchronization required	Low	Low
4 IDLE/1 non-IDLE	Low	High
Disparity-based IDLE sequence	High	Low
Align to special control character K28.3 (/A/)	High	High

The 4/1 IDLE sequence is defined as four consecutive IDLE code groups followed by a non-IDLE code group. The disparity-based IDLE sequence is 16 consecutive IDLE code groups with improper disparity on the second and third IDLE code group in the sequence. The disparity-based IDLE sequence is described further in Section 2.4.1, “Transmitting Uncoded Data—8-/4-Bit Modes.” Optionally the special control character K28.3 (/A/) may be used as a word synchronization event.

Word synchronization events must be generated at all concerned transmitters simultaneously in order for synchronization to be achieved. Word synchronization events must be received at all concerned receivers within 40 bit-times of each other.

Word synchronization events are used to establish a relationship between the received bytes in each of the receivers. The bytes of a word are matched and presented simultaneously at the receiver interface. Once synchronization is achieved the receiver tolerates $\pm$6 bit-times of drift between receivers. If drift exceeds $\pm$6 bit-times the receiver will continue to operate. However, the received bytes will no longer be synchronized properly because the receiver remains locked on the initially established synchronization. Word synchronization remains locked until one of three events occur that indicate loss of synchronization.

- Word synchronization lock is lost when one or more of the receivers lose or change byte alignment. Byte alignment loss is described in Section 3.5.2, “Byte-Aligned Mode (BSYNC = High).”
- Lock is also lost when overrun/underrun is detected on one or more of the receivers, see Section 3.6.2, “Reference Clock Timing Mode (RCCE = Low),” for more about overrun/underrun.
- Finally, both byte and word synchronization are lost when explicitly invalidated by asserting XCVR_*x*_DISABLE high. Word synchronization lock is lost when explicitly invalidated by asserting DROP_SYNC and XCVR_*x*_DISABLE high for at least two clocks (see Section 3.5.2, “Byte-Aligned Mode (BSYNC = High),” for details on performing drop sync).

When word synchronization is lost it must be re-established before data flow through the receiver resumes.

The receiver interface is disabled during initial word alignment. No data is produced at its outputs until word alignment is achieved and a word synchronization event has been detected. When establishing word synchronization, or when word synchronization is lost, ‘not word sync’ error is reported as described in Section 3.8.1, “Byte Mode (Uncoded Data).”

Word synchronization is possible in byte interface mode and TBI mode. However, word synchronization may be dependent on the detection of simultaneously transmitted word synchronization events that contain Idle characters. Therefore, if operating in TBI mode, either the Idle character must be a supported member of the code set or the ‘A’ character alignment must be used.

If WSE is high, then all enabled receivers (those that have XCVR_*x*_DISABLE negated low) will be aligned into a 16-, 24-, or 32-bit word (depending on the states of the various XCVR_*x*_DISABLE signals). If the receiver on channel A is disabled, then do not select the clock from channel A as the recovered clock for all the channels.

3.6 Receiver Interface Timing Modes

The receiver interface is timed to the recovered clock (link partner’s clock) or to the reference clock (local clock), depending on the state of the recovered clock enable, RCCE, signal. RCCE enables timing relative to the recovered clock when asserted and enables timing relative to the reference clock when negated.

The receiver interface clock signals, RECV_*x*_RCLK, will always be present when the PLL is in lock. This is true even if there is no signal present on the serial inputs or if the receiver has not achieved alignment or byte sync. The frequency of the receiver clock will be the local reference clock until synchronization is achieved. The RECV_*x*_RCLK clock signals, however, are not present during power up or when the MC92603 is in reset mode and the PLL is not locked.

All receiver channels data outputs are source synchronous with their respective RECV_*x*_RCLK outputs. They may be configured to be source aligned or source centered with their respective RECV_*x*_RCLK outputs. The configuration signal, RECV_CLK_CENT, when asserted high, will center the receiver clocks relative to the data and status outputs.

NOTE

The receiver clock complement, RECV_*x*_RCLK_B, is only provided in the TBIE/RTBI Ethernet compliant application modes (TBIE and COMPAT = high). If either TBIE or COMPAT is low, then RECV_*x*_RCLK_B is always low.

3.6.1 Recovered Clock Timing Mode (RCCE = High)

With RCCE asserted, the receiver clock signal, RECV_*x*_RCLK, is generated by the receiver and, on average, runs at the reference clock frequency of the transmitter (link partner’s clock) at the other end of the link. The recovered clock is not generated by a clock recovery PLL but by monitoring the receive FIFO.

When RCCE is high, the configuration signal, RECV_REF_A, is used to select the clock to be used. If RECV_REF_A is high, channel A's recovered clock is used for all four channels. If it is low, then each channel uses its own recovered clock. If RECV_REF_A is high, it is assumed that all four channels are operating at an identical frequency.

In order to track a transmitter frequency that is offset from the receiver's reference clock frequency, the duty cycle and period of the RECV_*x*_RCLK is modulated. For example, if the transmitter is sending data at a rate faster than the receiver, then a shortened cycle is generated as needed to track the incoming data rate. Alternately, if the transmitter is running slower than the receiver, then a long cycle is generated. The recovered clock duty cycle may be reduced or increased by 200 ps (if nominal frequency is 125 MHz) in order to match the transmitter frequency. For example, if the reference clock frequency is 125 MHz, this means that the minimum recovered clock cycle time is 7.8 ns and the maximum recovered clock cycle is 8.2 ns.

NOTE

Devices that interface to a MC92603 and are run in a recovered clock mode, must be able to tolerate this modulated clock.

When operating in the recovered clock timing mode, the addition or deletion of IDLEs is inappropriate. If RCCE is asserted (recovered clock timing mode), the add/delete IDLE enable, ADIE, signal must be low.

3.6.2 Reference Clock Timing Mode (RCCE = Low)

Data is timed relative to the local reference clock when RCCE is low. Synchronization between the recovered clock and the reference clock is handled by the receiver interface. Frequency offset between the transmitter's reference clock and the receiver's reference clock causes overrun/underrun situations. Overrun occurs when the link partner's transmitter is running faster than the receiver. Underrun occurs when the transmitter is running slower than the receiver. To avoid overrun/underrun conditions, rate adaption performed whereby, data is dropped or repeated to allow the data to be presented at the interface at the local reference clock frequency. Table 3-7 summarizes the rate adaption technique as a function of the receiver configuration when the receiver reference clock is slower than the transmitter reference clock. Table 3-8 summarizes the rate adaption technique as a function of the receiver configuration when the receiver reference clock is faster than the transmitter reference clock.

The ability to drop/repeat data is controlled by the ADIE configuration input. For instance, if ADIE is high and COMPAT is low, pairs of IDLE bytes (K28.5) will be dropped/repeated. If an overrun situation is imminent (transmitter is faster than the receiver), then the receiver interface searches for a pair of IDLE bytes to drop. Two consecutive IDLE bytes are dropped to assure that running disparity is not affected. If sufficient IDLE patterns are not available to drop, the receiver overrun may occur. When an overrun occurs, the 'overrun' error is reported as described in Table 3-12, Table 3-15, or Table 3-16 for a 1-byte clock period and 2 code groups of data are dropped. A sufficient number of IDLEs must be transmitted to guard against an overrun.

The frequency of IDLEs can be computed, based on the maximum frequency offset between the transmitter and receiver in the system. The number of bytes (code groups) that can be transmitted between a pair of IDLEs is:

$(2*10^6/N) - 1$ bytes, where N is the frequency offset in ppm.

Table 3-7. Receiver Reference Clock is Slower than Transmitter Reference Clock

ADIE	COMPAT	Receive Mode	Result	Action Taken
Low	Low	—	Overrun	2 bytes of data are lost. First byte reports overrun, second byte is skipped.
High	Low	—	Data dropped	2 consecutive IDLEs (K28.5) are dropped
High	Low	Auto-negotiate sequence	Data dropped	16 bytes dropped (/C1/C2/C1/C2/)
High	High	Idle sequence	Data dropped	2 bytes dropped (/I2/)

In an underrun situation, data must be repeated in order to maintain synchronization between the clock domains. If ADIE is high and COMPAT is low, the receiver interface will repeat a pair of IDLE bytes when underrun is imminent. This allows the user to establish ‘packets’ of data that do not contain IDLEs and the MC92603 will not insert IDLEs in the middle of these ‘packets.’ The IDLE frequency to prevent underrun is identical to the frequency to prevent overrun, so the same conditions apply.

If an underrun occurs, the ‘underrun’ error is reported as described in Table 3-12, Table 3-15, or Table 3-16 for a 1-byte clock period and 2 bytes of data are repeated.

Table 3-8. Receiver Reference Clock is Faster than Transmitter Reference Clock

ADIE	COMPAT	Receive Mode	Result	Action Taken
Low	Low	—	Underrun	2 bytes of data are lost. First byte reports underrun, second byte repeats byte prior to underrun.
High	Low	—	Data repeated	2 consecutive IDLEs (K28.5) are repeated
High	High	Auto-negotiate sequence	Data repeated	16 bytes repeated (/C1/C2/C1/C2/)
High	High	Idle sequence	Data repeated	2 bytes repeated (/I2/)

NOTE

When operating in ‘word’ mode both channels must add/delete IDLEs simultaneously. IDLEs must appear in the data stream for both channels simultaneously, so that IDLEs may be repeated or deleted.

3.7 Ethernet Compliant Applications Modes (COMPAT = High)

The following sections discuss Ethernet compliant applications modes as implemented by the MC92603. Different Ethernet operations and protocols as described in the IEEE Std. 802.3-2002 specification [4], are also discussed.

3.7.1 Interface to Ethernet MAC

The operation of the transceivers in the Ethernet-compatible GMII and TBI modes and the correlation of the port signal names to the names in the **IEEE Std. 802.3-2002** specification [4] are listed in the following two sections.

3.7.1.1 GMII Operation

Ethernet GMII mode is enabled by negating the TBIE input as low and asserting the COMPAT input high. When in this mode, the receiver should be connected to a standard Gigabit Ethernet MAC, as shown in Table 3-9.

Table 3-9. GMII Connection to Standard Ethernet MAC

IEEE Std. 802.3-2002 Signal Name	Function	Direction (Relative to MC92603)	Port Name
GTX_CLK	Transmit clock	Input	XMIT_*x*_CLK
TX_EN	Transmit enable	Input	XMIT_*x*_ENABLE
TX_ER	Force error on transmitted byte	Input	XMIT_*x*_ERR
TXD<7:0>	Transmit data	Input	XMIT_*x*_7:0]
RX_CLK	Receive clock	Output	RECV_*x*_RCLK
RXD<7:0>	Receive data	Output	RECV_*x*_[7:0]
RX_ER	Receiver has detected an error	Output	RECV_*x*_ERR
RX_DV	Receiver has detected data	Output	RECV_*x*_DV
MDC	Management data clock	Input	MD_CLK
MDIO	Management data input/output	Bidirectional	MD_DATA
The following MAC half-duplex input must be externally pulled up/down as indicated			
COL	Receiver has sensed a collision	Pull down	—
CRS	Receiver has sensed a carrier	—	—
The following MC92603 inputs must be externally pulled up/down as indicated			
Pull up	Management interface enable	Input	MDIO_EN
Variable (PUP/PUD)	MDIO PHY address	Input	MD_ADR[4:2]
Pull down	Disable unused transmitter input	Input	XMIT_*x*_K
Pull down	Configuration input—put in 8-bit mode	Input	TBIE
Pull up	Configuration input—put in byte synchronized mode	Input	BSYNC
Pull down	Configuration inputs—disable word alignment	Input	WSYNC1 and WSYNC0

Initially, the receiver must attain byte alignment through the detection of four COMMA code groups with the same alignment as explained in Section 3.5.1, “Non-Aligned Mode (BSYNC = Low).” Next, the receiver must attain stream alignment as described and shown in Figure 36-9 of the **IEEE Std. 802.3-2002 specification [4]**.

The RECV_*x*_ERR output remains high until both alignments are attained.

The receiver then searches for a Start_of_Packet code group (/S/). On detection of a Start_of_Packet, the receiver replaces that code group with a preamble code group (0x55) and present this data on the receiver data output REC_*x*_7 through RECV_*x*_0 as the RECV_*x*_DV output is raised. This is per Figures 36-7a and 36-7b of **IEEE Std. 802.3-2002 specification [4]**.

Data continues to be presented on the data outputs, and the RECV_*x*_DV output remains high until an End_of_Packet code group (/T/) is received. At this point the RECV_*x*_DV output is negated low and remains low until the next Start_of_Packet is received.

When operating in GMII mode, the receiver status is reported by RECV_*x*_ERR and RECV_*x*_DV and encoded on the RECV_*x*_[7:0] data signals, as shown in Table 3-10.

Table 3-10. Receiver Status in GMII Mode

RECV_*x*_ ERR	RECV_*x*_ DV	RECV_*x*_ RCLK_B	RECV_*x*_ [7:0]	Description
High	Low	Low	0x00	Not byte sync: The receiver is in start-up or has lost byte alignment and is searching for alignment.
Low	Low	Low	Don't care	Normal inter-frame gap
Low	High	Low	Data	Normal operation, valid data code group received.
High	High	Low	0x20	Error propagation
High	High	Low	0x10	Disparity error
High	High	Low	0x08	Code error
High	High	Low	0x04	Overrun
High	High	Low	0x02	Underrun

3.7.1.2 TBI Operation

The Ethernet TBI interface is enabled by asserting the TBIE and COMPAT inputs high. When in this mode, the MC92603 will conform to the IEEE Std. 802.3-2002 TBI interface signals and protocol. The complete TBI connection to a standard Ethernet MAC is shown in Table 3-11. Note that MDIO is available for use when not in GMII mode.

Table 3-11. TBI Connection to Standard Ethernet MAC

IEEE Std. 802.3-2002 Signal Name	Function	Direction (Relative to MC92603)	Port Name
PMA_TX_CLK	Transmit clock	Input	XMIT_*x*_CLK
tx_code_group<9:0>	Transmit data	Input	XMIT_*x*_ERR, XMIT_*x*_ENABLE, XMIT_*x*_[7:0]
EWRAP	Enable data wraparound	Input	XMIT_*x*_LBE
EN_CDET	Enable COMMA detect	Input	XMIT_*x*_K
COM_DET	Receiver detected a COMMA	Output	RECV_*x*_COMMA
rx_code_group<9:0>	Receive data	Output	RECV_*x*_ERR, RECV_*x*_DV, RECV_*x*_[7:0]
-LCK_REF	Enable lock to reference	Input	RCCE (normally low, affects all 4 channels)
PMA_RX_CLK<0:1>	Receive clocks (both phases)	Output	RECV_*x*_RCLK, RECV_*x*_RCLK_B
The following output is available, but is not a standard TBI signal:			
—	Receiver detected an error	Output	RECV_*x*_K
The following inputs must be externally pulled up/down as indicated:			
Pull up	Management interface enable	Input	MDIO_EN
Variable (PUP/PUD)	MDIO PHY address	Input	MD_ADR[4:2]
Pull up	Configuration	Input	TBIE
Pull up	Configuration	Input	BSYNC

The receiver interface works similar to the backplane 10-bit mode, except that word synchronization is not supported and a non-aligned operation is not allowed. Also, in this mode, the XMIT_*x*_K input is not

required for the transmitter, so it is used to ‘enable COMMA detect.’ Data out of the receiver is even-/odd-aligned with the two output clocks. COMMAs are initially aligned with the rising edge of RECV_*x*_RCLK_B. The MC92603 will always initially perform even/odd alignment to the first COMMA (K28.1, K28.5, or K28.7) code group encountered. If XMIT_*x*_K is low, it will not realign to any future COMMAs that may appear in the data stream. If ‘enable COMMA detect’ is enabled (XMIT_*x*_K is high), a data code group may be repeated to force this alignment if an IDLE is encountered in an ODD code group.

The receiver interface error and status in TBI mode is shown in Table 3-12.

Table 3-12. Receiver Interface Error and Status Codes (TBI Mode)

RECV_*x*_K[1]	RECV_*x*_COMMA	RECV_*x*_ERR	RECV_*x*_DV	RECV_*x*_[7:0]	Priority[2]	Description
Low	Low	Data[9]	Data[8]	Data[7:0]	6	Normal operation, non-COMMA code group received.
Low	High	Data[9]	Data[8]	Data[7:0]	5	Normal operation, COMMA (K28.1, K28.5, or K28.7) code group received.
High	Don’t care	Don’t care	Don’t care	0x04	3	Overrun
High	Don’t care	Don’t care	Don’t care	0x02	3	Underrun
High	Don’t care	Don’t care	Don’t care	0x00	1	Not byte sync: the receiver is in start-up or has lost byte alignment and is searching for alignment.

1 RECV_*x*_K is not a standard TBI signal. These errors may be detected by monitoring only the10-bit data field since the 3 error codes are not valid 10-bit encoded data.

2 The priority column shows the error that is reported if multiple errors occur at the same time. The lower numbered priority errors are reported first.

3.7.1.3 Double Data Rate Operation—RGMI and RTBI

Functionally, the double data rate operation (DDR is high) is identical to the previously mentioned receiver GMII and TBI operating modes. The only difference is at the chip parallel data interfaces. Data outputs are shared and defined uniquely, depending on each phase of the output clock (RECV_*x*_RCLK). The RGMII and RTBI interfaces are shown in Table 3-13 and Table 3-14, respectively.

Table 3-13. Receiver RGMII Interface

Clock Edge	RECV_*x*_DV	RECV_*x*_[3:0]
Rising	RX_DV	Data bit [3:0]
Falling	GMII_RX_ER (XOR) GMII_RX_DV	Data bit [7:4]

Table 3-14. Receiver RTBI Interface

Rising Edge of Clock	RECV_*x*_COMMA	RECV_*x*_DV	RECV_*x*_[3:0]
RECV_*x*_RCLK	COM_DET	Data bit 4	Data bit [3:0]
RECV_*x*_RCLK_B	COM_DET	Data bit 9	Data bit [8:5]

3.7.2 Rate Adaption of Ethernet Packet Data Streams

The MC92603 supports applications in which the device is used to transmit and receive **IEEE Std. 802.3-2002**, PCS, PMA, type 1000BASE-X packet streams. When the MC92603 is being operated in reference clock mode, as described in Section 3.6.2, "Reference Clock Timing Mode (RCCE = Low)," rate adaption is performed to account for frequency offset between the transmitter and receiver. In backplane applications (see Section 3.6.2, "Reference Clock Timing Mode (RCCE = Low)"), rate adaption is accommodated by adding K28.5 IDLE code groups to, or deleting K28.5 IDLE code groups from, the data stream to match the incoming data rate to the receiver data rate as defined by its reference clock frequency. The indiscriminate addition or deletion of K28.5 IDLE code groups from an 802.3 packet stream would interfere with proper system operation.

The MC92603 compatibility mode (COMPAT input is high) allows for rate adaption using methods compatible with Ethernet packet streams and does not interfere with proper system operation. The following are the features of the compatibility mode:

- Context-sensitive rate adaption during receipt of configuration, IDLE, and data code groups
- Tolerates up to ±100 ppm frequency offset
- Supports Jumbo frame lengths of up to 14 Kbytes (if JPACK is high)
- Supports frame bursting
- Internal or external 8B/10B encoding/decoding may be used
- Compatible with **IEEE Std. 802.3-2002** Clause 4 specification [4] of media access control function
- Compatible with Clause 36 of the specification [4] of physical coding sublayer (PCS) and physical medium attachment (PMA) sublayer function
- Compatible with Clause 37 of the specification [4] of auto-negotiation function

3.7.2.1 Rate Adaption Method

The MC92603 utilizes a FIFO in its receiver to act as an elastic buffer for the receive data interface. The elastic buffer allows for proper operation of the interface in the presence of jitter and frequency offset. However, frequency offset will eventually lead to elastic buffer overrun or underrun. In order to prevent underruns and overruns, one or more code groups must be added to or deleted from the packet stream.

The MC92603 must determine the proper type of code groups to add or delete and do it at an appropriate time to ensure compatibility with the packet data streams. The code group type and timing is determined by the current context of the packet stream. There are three contexts considered: configuration, idle, and data transmission.

3.7.2.2 Configuration Context

The configuration context is when the transceivers are transmitting configuration ordered sets in support of auto-negotiation. A configuration ordered set consists of alternating /C1/ and /C2/ code group sets as shown below:

/C1/: /K28.5/D21.5/Dxx.x/Dxx.x

/C2/: /K28.5/D2.2/Dxx.x/Dxx.x

where /Dxx.x/Dxx.x/ represent the 16-bit contents of the configuration register. During auto-negotiation alternating /C1/ and /C2/ code group sets are expected and the duration of the auto-negotiation sequence is not bounded. Therefore, rate adaption is accomplished through the addition and deletion of /C1/ and /C2/ code group sets.

On detection of an imminent overflow, the MC92603 searches for and deletes two /C1/C2/ code group sets, removing a total of 16 code groups from the packet stream. The auto-negotiation function can tolerate missing two complete sets because of its handshaking protocol. Two complete /C1/C2/ code groups sets must be deleted, because, for a constant configuration register value, a single /C1/C2/ code group set toggles running disparity. Removing two /C1/C2/ code group sets maintains proper running disparity.

On detection of an imminent underflow, searches for two adjacent /C1/C2/ code group sets with a constant configuration register value and inserts a copy of them into the packet stream, adding a total of 16 code groups. The auto-negotiation function is tolerant of additional valid sets because of its handshaking protocol. In order to maintain proper running disparity as described above, two complete /C1/C2/ code group sets must be added to the packet stream.

3.7.2.3 Idle Context

The idle context is when the transceivers are transmitting idle ordered sets while the link is idle or during inter-packet gaps (IPG). An idle ordered set consists of two types of code group pairs:

/I1/: /K28.5/D5.6

/I2/: /K28.5/D16.2

where /I1/ is a correcting idle and /I2/ is a preserving idle. The rules for the insertion of idle ordered sets into a packet stream dictate that the resulting running disparity be negative after the idle code group is inserted. A correcting idle, /I1/, toggles positive running disparity to negative; a preserving idle, /I2/, maintains negative running disparity. These rules are in place specifically to allow the addition or deletion of preserving idle ordered sets by repeaters to accommodate retiming. Rate adaption in the idle context is accomplished through the addition and deletion of preserving idle (/I2/) ordered sets.

On detection of an imminent overflow, the MC92603 searches for and deletes an /I2/ ordered set, removing a total of two code groups from the packet stream. The packet stream tolerates deletion of /I2/ as described above. Deleting /I2/ raises concerns about IPG shrinkage. The IPG on transmit is required to be at least 12 code groups in duration, including the end of packet delimiter (EPD). The received IPG is only required to be at least eight code groups in duration, leaving four code groups available to remove per IPG.

NOTE

The MC92603 does not verify that the IPG meets minimum length requirements after removal of the /I2/ code groups. It assumes that the IPG has at least 12 code groups in length when received.

On detection of an imminent underflow, the MC92603 searches for an /I2/ ordered set and repeats an /I2/ in the packet stream, adding a total of two code groups. The packet stream tolerates additional /I2/ ordered sets because maximum IPG length is not limited.

Special consideration is given to IPG in the data context to accommodate Jumbo frames and frame bursting. These are described in the next section.

3.7.2.4 Data Context

The data context is when the transceivers are transmitting data frames encapsulated into code group packets. The code groups in the packet cannot be disturbed, therefore, rate adaption is accomplished in the IPG as described above.

On detection of an imminent overflow, the MC92603 searches for and deletes an /I2/ ordered set, removing a total of two or four code groups from the IPG.

On detection of an imminent underflow, the MC92603 searches for a /I2/ ordered set and inserts an /I2/ adjacent to it into the IPG, adding a total of two code groups.

A special case that must be considered in the data context is Jumbo frames. Jumbo frames are not supported in the standard but are rather a defacto-standard. Jumbo frames violate the untagged maximum frame size of 1518 code groups and increases the size to 14K code groups. Given a maximum total frequency offset of 200 ppm, a Jumbo frame could lead to a surplus or deficit of 3.0 code groups for which rate adaption must account.

The depth of the receivers elastic buffers may be increased by asserting JPACK in order to ensure against starvation in the presence of Jumbo frames. This increase will lead to longer receiver latency.

3.7.3 Error Handling

The receiver interface error reporting mechanisms as described in Section 3.7.1.2, “TBI Operation,” and Table 3-11 are used in the compatibility mode with one further definition; overrun/underrun errors are processed specially.

Overrun may occur when an appropriate code group to remove cannot be identified. In this situation, one code group is replaced in the data stream (to report the error), and a second data code group is removed from the packet stream. The received packet stream continues normally thereafter. The MAC sublayer should detect the repeated code group as a CRC error.

Underrun may occur when an appropriate code group to insert cannot be identified. In this situation, one data code group is repeated in the packet stream. The received packet stream continues normally thereafter. The repeated code group is reported as an underrun error as described in Section 3.7.1.2, “TBI Operation,” and Table 3-11. The MAC sublayer should detect the repeated code group as a CRC error.

3.7.3.1 Jumbo Frame Considerations

It is recommended if Jumbo frames are to be supported, that the ‘recovered clock mode’ (RCCE is high) be used to reduce power and latency. It should be noted that it is possible for the MC92603 transmit controller to shorten the IPG by two to achieve even/odd alignment and for the receiver to remove four code groups in the IPG to perform rate adaption if in ‘reference clock mode.’ This means that if the IPG is only 12 code groups originally, then the receiver could present an IPG as small as 6 code groups (with maximum frequency offset).

If at least eight code groups are required in the IPG in the user's application the alternatives are the following:

- Run in 'recovered clock mode'
- Furnish an initial IPG of at least 14 code groups
- Ensure that the total of the frequency offset and packet length does not require more than two code groups to be deleted
- Maximum number of code groups dropped per packet = frequency offset * packet length

3.8 Backplane Applications Modes (COMPAT = Low)

3.8.1 Byte Mode (Uncoded Data)

Backplane byte mode is enabled by negating both the TBIE and COMPAT signals low. The received data is a byte (8 bits) of data when in this mode. The internal 8B/10B decoder is used to decode the 8-bit data from the 10-bit code group received. The received byte is presented on the RECV_*x*_7–RECV_*x*_0 signals.

The RECV_*x*_ERR is negated low when the receiver is operating normally and asserted high when received data contains an error or the receiver is in an error state. When RECV_*x*_ERR is high, the state of the RECV_*x*_7–RECV_*x*_0 signals are decoded to determine the error condition. Table 3-15 describes the error codes and their meaning.

The receiver interface is always timed to the output clock, RECV_*x*_RCLK. This clock may be derived from the receiver's recovered clock or to the reference clock depending on the state of the RCCE signal as previously discussed.

Table 3-15. Receiver Interface Error and Status Codes (Backplane Byte Mode)

RECV_*x*_ ERR	RECV_*x*_ DV	RECV_*x*_ K	RECV_*x*_ COMMA	RECV_*x*_ [7:0]	Priority[1]	Description
Low	Low	Don't care	Don't care	Don't care		Undefined for backplane byte mode
Low	High	Low	Don't care	Data	9	Normal operation, valid data code group received.
Low	High	High	Low	Data	8	Normal operation, special code group (non-COMMA) detected.
Low	High	High	High	Data	7	Normal operation (COMMA detected)
High	Don't care	Don't care	Don't care	0x10	6	Disparity error: The 8B/10B decoder detected a disparity error.
High	Don't care	Don't care	Don't care	0x08	5	Code error: The 8B/10B decoder detected an illegal code group.
High	Don't care	Don't care	Don't care	0x04	3	Overrun
High	Don't care	Don't care	Don't care	0x02	3	Underrun
High	Don't care	Don't care	Don't care	0x01	2	Not word sync: The receiver is byte synchronized but has not achieved or has lost word alignment and is searching for alignment.

Table 3-15. Receiver Interface Error and Status Codes (Backplane Byte Mode) (continued)

RECV_*x*_ ERR	RECV_*x*_ DV	RECV_*x*_ K	RECV_*x*_ COMMA	RECV_*x*_ [7:0]	Priority[1]	Description
High	Don't care	Don't care	Don't care	0x00	1	Not byte sync: The receiver is in start-up or has lost byte alignment and is searching for alignment.

1 The priority column shows the error that is reported if multiple errors occur at the same time. The lower priority-numbered errors are reported first.

3.8.2 10-Bit Mode (Coded Data)

Backplane 10-bit mode is enabled by asserting TBIE high and negating COMPAT low, as shown in Table 3-15.

Received data is 10 bits of coded data. The internal 8B/10B decoder is bypassed. Receiver data is presented on the signals: RECV_*x*_ERR, RECV_*x*_DV, and RECV_*x*_7–RECV_*x*_0 (making up bits 9–0, respectively).

The RECV_*x*_COMMA is asserted high whenever the 10-bit code group is 1 of the 3 COMMA code groups.

The RECV_*x*_K is asserted high when the receiver is in an error state. When RECV_*x*_K is high, the state of the RECV_*x*_7–RECV_*x*_0 signals are decoded to determine the error condition.

The receiver interface is timed to the clock output, RECV_*x*_RCLK.

Table 3-16. Receiver Interface Error and Status Codes (Backplane 10-Bit Mode)

RECV_*x*_ K	RECV_*x*_ COMMA	RECV_*x*_ ERR	RECV_*x*_ DV	RECV_*x*_ [7:0]	Priority[1]	Description
Low	Low	Data[9]	Data[8]	Data[7:0]	6	Normal operation, non-COMMA code group received.
Low	High	Data[9]	Data[8]	Data[7:0]	5	Normal operation, COMMA (K28.1, K28.5, or K28.7) code group received.
High	Don't care	Don't care	Don't care	0x04	3	Overrun
High	Don't care	Don't care	Don't care	0x02	3	Underrun
High	Don't care	Don't care	Don't care	0x01	2	Not word sync: The receiver is in start-up or has lost word alignment and is searching for alignment.
High	Don't care	Don't care	Don't care	0x00	1	Not byte sync: The receiver is in start-up or has lost byte alignment and is searching for alignment.

1 The priority column shows the error that is reported if multiple errors occur at the same time. The lower priority numbered errors are reported first.

3.8.2.1 Double Data Rate Operation—Backplane Applications

When configured for backplane applications (COMPAT = low), double data rate operation (DDR high) is functionally identical to the previously mentioned receiver operating modes. The difference is only at the chip parallel data interfaces. Data outputs are shared and defined uniquely depending for each phase of the output clock (RECV_*x*_RCLK).

The double data rate interfaces for receiving uncoded or coded data are shown in Table 3-17 and Table 3-18, respectively.

Table 3-17. DDR Backplane Uncoded Data (8-Bit Mode)

Clock Edge	RECV_*x*_K	RECV_*x*_COMMA	RECV_*x*_DV	RECV_*x*_[3:0]
Rising	RECV_*x*_K	RECV_*x*_COMMA	RECV_*x*_DV	Data bit [3:0]
Falling	RECV_*x*_K	RECV_*x*_COMMA	RECV_*x*_ERR (XOR) RECV_*x*_DV	Data bit [7:4]

Table 3-18. DDR Backplane Coded Data (10-Bit Mode)

Clock Edge	RECV_*x*_K	RECV_*x*_COMMA	RECV_*x*_DV	RECV_*x*_[3:0]
Rising	RECV_*x*_K	RECV_*x*_COMMA	Data bit 4	Data bit [3:0]
Falling	RECV_*x*_K	RECV_*x*_COMMA	Data bit 9	Data bit [8:5]

Chapter 4
Management Interface (MDIO)

This chapter consists of the following sections:

- Section 4.1, “MDIO Interface”
- Section 4.2, “MDIO Registers”

The management data input/output (MDIO) interface as defined in Clause 22 of **IEEE Std. 802.3-2002 [4]** is supported by the MC92603 Quad Gigabit Ethernet transceiver. Details for protocol and electrical characteristics are available in the standard.

This chapter provides details on the MDIO interface signals and their associated registers. The MDIO is accessible in all of the backplane or Ethernet compatibility operational modes.

4.1 MDIO Interface

The MC92603 chip MDIO interface consists of one enable input, five address inputs, one clock input, and one bidirectional data signal.

Some users may wish to use the MDIO interface, and others may not. If the MDIO interface is to be used then the MDIO enable input, MDIO_EN, must be asserted high. The MDIO interface is available whether COMPAT is enabled or not.

On power up, the MC92603 will always assume the default configuration defined by the pins of the device. The configuration can then be changed through the MDIO interface regardless of the application operating mode. If MDIO is not used (MDIO_EN is low), the MC92603 will operate in the default configuration.

The MDIO interface is a multidrop serial interface and each part must have a unique PHY address. Each channel is addressed separately in the MC92603. The base address to each transceiver must be mod 4. This address is read from three input pins that must be externally pulled up or pulled down to furnish a unique address for each part that is connected to a MDIO bus. These three address inputs are identified as: MD_ADR4, MD_ADR3, and MD_ADR2.

The 2 least significant bits of the 5-bit address, MD_ADR1 and MD_ADR0, are used to uniquely identify each MC92603 channel (00 indicates channel A, 01 = B, 10 = C, and 11 = indicates channel D).

The 2.5-MHz data interface clock, MD_CLK, is sourced at the MDIO master (MAC) and is used by each slave MDIO device. The MC92603 is designed as MDIO slave devices.

The MDIO data signal, MD_DATA, is a bidirectional serial signal used to read and write management data from/to the MDIO registers.

4.2 MDIO Registers

The specification calls for up to 64 registers to be supported by MDIO. Some registers must be included to meet the minimum MDIO specification; they are identified as the basic register set. Other registers are optional and are considered part of the extended register set. The MC92603 has four sets of MDIO registers (one per transceiver channel). Registers for address 0–6 and 15–18, as defined in the standard specification, are fully supported. Registers 7–14 and 19–31 are not supported in the MC92603. The MDIO registers are identified in Table 4-1.

Table 4-1. MDIO Management Register Set

MDIO Register Address (RA)	Register Name	Basic/Extended Register Set	Supported by MC92603
0	Control	B	Yes
1	Status		
2, 3	PHY identifier	E	
4	Auto-negotiation advertisement		
5	Auto-negotiation link partner base page ability		
6	Auto-negotiation expansion		
7	Auto-negotiation next page transmit		No
8	Auto-negotiation link partner received next page		
9	Master-slave control register		
10	Master-slave status register		
11–14	Reserved		
15	Extended status	B	Yes
16	Vendor specific—permanent configuration control	E	
17	Vendor specific—channel configuration and status		
18	Vendor specific—BERT error counter		
19–31	Vendor specific—not implemented		No

4.2.1 MDIO RA 0—Control Register

Figure 4-1 shows the format for the control register, MDIO RA 0, in the MC92603.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PHY Reset	Loop-back	Speed Select [0]	Auto-Negotiation Enable	Power Down	Isolate	Restart Auto-Negotiation	Duplex Mode	Collision Test	Speed Select [1]	Reserved					
W																
Reset	1/0	XCVR_ *x*_LBE	0	ENABLE_AN	0	0	0	1	0	1	0	0	0	0	0	0

Figure 4-1. Control Register (MDIO RA 0)

Table 4-2 lists the corresponding field descriptions for the control register.

Table 4-2. Control Register (MDIO RA 0) Field Descriptions

Bits	Name	Description[1]
15	Reset	Bit 15 may be written through the MDIO interface. It is initialized to zero on power up or a device reset. When set, it forces the other MDIO registers to be loaded with their default value. This bit is automatically reset (self-clearing) one clock after it is set. (R/W, SC)
14	Loopback	Initialized to the value on the XCVR_x_LBE input. When set, it forces a digital loopback on the transceiver interface. When a channel is in loopback mode, data transmitted into the transmit interface is looped back on the serial link input to the same channel's receiver. (R/W)
13	Speed select [0]	Bit 13 is forced to zero and may not be modified. MC92603 is always configured as a 1-gigabit device. (R)
12	Auto-negotiation enable	Bit 12 is initialized to the value on the ENABLE_AN input, but may be modified through the MDIO interface. (R/W)
11	Power down	Bit 11 is forced to zero and may not be modified. MC92603 does not support power down. (R)
10	Isolate	Bit 10 is forced to zero and may not be modified. MC92603 does not support isolation of the GMII interface through the MDIO interface. Such isolation is available through the JTAG controller. (R)
9	Restart auto-negotiation	Bit 12 is initialized to zero but may be modified. If set, the auto-negotiation sequence is started (re-started). (R/W)
8	Duplex mode	Bit 8 is forced to one and may not be modified. MC92603 always runs in full-duplex mode. (R)
7	Collision test	Bit 7 is forced to zero and may not be modified. MC92603 does not run in half-duplex mode and, therefore, does not detect collisions. (R)
6	Speed select [1]	Bit 6 is forced to one and may not be modified. MC92603 is always configured as a 1-gigabit device. (R)
5–0	Reserved	Bits 5–0 are unused in the MC92603 application. They may not be modified. (R)

[1] R = read-only, R/W = read and write, and SC = self-clearing.

4.2.2 MDIO RA 1—Status Register

Figure 4-2 shows the format for the status register, MDIO RA 1, in the MC92603. The status register is a read-only register.

	15	14	13	12	11	10	9	8
R	100BASE-T4	100BASE-X Full-Duplex	100BASE-X Half -Duplex	10 Mb/s Full-Duplex	10 Mb/s Half-Duplex	100BASE-T2 Full-Duplex	100BASE-T2 Half-Duplex	Extended Status
W								
Reset	0	0	0	0	0	0	0	1

	7	6	5	4	3	2	1	0
R	Reserved	MF Preamble Suppress	Auto-Negotiation Complete	Remote Fault	Auto-Negotiation Ability	Link Status	Jabber Detect	Extended Capability
W								
Reset	0	0	0/1	0/1	0/1	0	0	1

Figure 4-2. Status Register (MDIO RA 1)

Table 4-3 lists the corresponding field descriptions for the status register.

Table 4-3. Status Register (MDIO RA 1) Field Descriptions

Bits	Name	Description[1]
15	100BASE-T4	Bit 15 is forced to zero and may not be modified. MC92603 does not support 100BASE-T4 operation. (R)
14	100BASE-X full-duplex	Bit 14 is forced to zero and may not be modified. MC92603 does not support 100BASE-X operation. (R)
13	100BASE-X half -duplex	Bit 13 is forced to zero and may not be modified. MC92603 does not support 100BASE-X operation. (R)
12	10 Mb/s full-duplex	Bit 12 is forced to zero and may not be modified. MC92603 does not support 100BASE-10 Mb/s operation. (R)
11	10 Mb/s half-duplex	Bit 11 is forced to zero and may not be modified. MC92603 does not support 100BASE-10 Mb/s operation. (R)
10	100BASE-T2 full-duplex	Bit 10 is forced to zero and may not be modified. MC92603 does not support 100BASE-T2 operation. (R)
9	100BASE-T2 half-duplex	Bit 9 is forced to zero and may not be modified. MC92603 does not support 100BASE-T2 operation. (R)
8	Extended status	Bit 8 is forced to one and may not be modified. MC92603 supports extended status operation. Extended status information is available in MDIO RA 15. (R)
7	Reserved	Bit 7 is forced to zero and may not be modified. (R)
6	MF preamble suppression	Bit 6 is forced to zero and may not be modified. The MC92603 implementation of the MDIO protocol requires a preamble for the management frames. (R)
5	Auto-negotiation complete	Bit 5 is initialized to zero This bit is set when the channel has successfully completed the AN sequence. This bit is cleared when read. (R, SC)

Table 4-3. Status Register (MDIO RA 1) Field Descriptions (continued)

Bits	Name	Description[1]
4	Remote fault	Bit 4 is initialized to zero and is set when the receiver detects a remote fault. (R, LH, SC)
3	Auto-negotiation ability	Bit 3 reports the AN ability per register 0.12. It may be changed via register 0.12 through the MDIO interface. (R)
2	Link status	Bit 2 is initialized to zero. It reflects whether the receiver has achieved byte synchronization. (R)
1	Jabber detect	Bit 1 is forced to zero and may not be modified. (R)
0	Extended capability	Bit 0 is forced to one and may not be modified. The MC92603 has a specific status and configuration register (register 17) for each channel. (R)

[1] R = read only, LH = latches high, and SC = self-clearing.

4.2.3 MDIO RA 2 and 3—PHY Identifier Registers

Figure 4-3 shows the format for the PHY identifier registers in the MC92603. MDIO RAs 2 and 3 are read-only and contain a 32-bit pattern that uniquely identifies the MC92603. They provide bits 3–24 of Freescale's 'organizational unique identifier' (0x000A28), the 6 least significant bits (lsb) of the part number and the revision level for the MC92603.

Register		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2	R	Bits 03–18 of OUI															
	W																
	Reset	0	1	0	1	0	0	0	1	0	1	0	0	0	0	0	0

Register		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	R	Bits 19–24 of OUI						Manufacturer's Model #						Revision			
	W																
	Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Figure 4-3. PHY Identifier Registers (MDIO RA 2 and 3)

4.2.4 MDIO RA 4—Auto-Negotiation Advertisement Register

Figure 4-4 shows the format for the auto-negotiation (AN) advertisement register, MDIO RA 4, in the MC92603.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Next Page	Acknowledge	Remote Fault 2	Remote Fault 1	Reserved			Pause 2	Pause 1	Half-Duplex	Full-Duplex	Reserved				
W																
Reset	0	0	1/0	1/0	0	0	0	0/1	0/1	0	1	0	0	0	0	0

Figure 4-4. Auto-Negotiation (AN) Advertisement Register (MDIO RA 4)

NOTE

The ‘Ack’ bit is set when three consecutive matching configuration registers are received. The auto-negotiation state is complete when three consecutive matching configuration registers are received with the ‘Ack’ bit set. The transmitter will continue sending auto-negotiation sequences once the auto-negotiation sequence is complete for at least 10 ms.

Table 4-4 lists the corresponding field descriptions for the AN advertisement register.

Table 4-4. AN Advertisement Register (MDIO RA 4) Field Descriptions

Bits	Name	Description[1]
15	Next page	Forced to zero. The MC92603 does not support multiple pages of configuration registers. (R)
14	Acknowledge	Ack—is set when the receiver detects a valid configuration from the link partner’s transmitter. (R)
13	Remote fault 2	Bits 13 and 12 are remote faults as detected by the receiver. (R)
12	Remote fault 1	
11–9	Reserved	Forced to zero and may not be modified. (R)
8	Pause 1	PS1 and PS2—Pause control bits that are modified through the MDIO interface by MAC. (R/W)
7	Pause 0	
6	Half-duplex	Forced to zero. The MC92603 does not support half-duplex mode. (R)
5	Full-duplex	Forced to one. The MC92603 always runs in full-duplex mode. (R)
4–0	Reserved	Forced to zero and may not be modified. (R)

RF1	RF2	Interpretation
0	0	Link is okay
0	1	Offline (XCVR_*x*_DISABLE is high)
1	0	Link failure (receiver is not byte-synced)
1	1	Link failure during auto-negotiation (receiver is not byte-synced during the auto-negotiation sequence)

[1] R = read-only, R/W = read and write.

4.2.5 MDIO RA 5—Auto-Negotiation Link Partner Ability Register

Figure 4-5 shows the format for the auto-negotiation (AN) link partner register, MDIO RA 5, in the MC92603. Register 5 is a read-only register and contains the advertised ability of the link partner.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Next Page	Acknowledge	Remote Fault 2	Remote Fault 1	Reserved			Pause 2	Pause 1	Half-Duplex	Full-Duplex	Reserved				
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-5. AN Link Partner Ability Register (MDIO RA 5)

Table 4-5 lists the corresponding field descriptions for the AN link partner ability register.

Table 4-5. AN Link Partner Ability Register Field Descriptions

Bits	Name	Description[1]
15	Next Page	The MC92603 does not support multiple pages of configuration registers and ignores this bit. (R)
14	Acknowledge	Ack is set when the link partner acknowledges receipt of the advertised transmitted capabilities. (R)
13	Remote fault 2	Bits 13 and 12 are the remote status of the link partner. (R) RF1 / RF2 / Interpretation: 0 / 0 / Link OK 0 / 1 / Offline 1 / 0 / Link_Failure 1 / 1 / Auto-Negotiation_Error
12	Remote fault 1	
11–9	Reserved	This bit is ignored. (R)
8	Pause 1	PS1 and PS2 are pause control bits that reflect the values of bits 12 and 13 in MDIO RA 4 of the link partner. (R)
7	Pause 0	
6	Half-duplex	Forced to zero. The MC92603 does not support half-duplex mode. (R)
5	Full-duplex	Forced to one. The MC92603 always runs in full-duplex mode. (R)
4–0	Reserved	This bit is ignored. (R)

[1] R = read-only.

4.2.6 MDIO RA 6—Auto-Negotiation (AN) Expansion Register

Figure 4-6 shows the format for the auto-negotiation (AN) expansion register, MDIO RA 6, in the MC92603. All bits of register 6 are read-only and the register contains data received from the link partner.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved													Next Page Enable	Page Received	Reserved
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-6. AN Expansion Register (MDIO RA 6)

4.2.7 MDIO RA 7–14—Not Supported

MDIO RA 7–14 registers, as shown in Table 4-1, are not supported in the MC92603 PHY.

4.2.8 MDIO RA 15—Extended Status Register

Figure 4-7 shows the content of the extended status register, MDIO RA 15, and its state for the MC92603. The register is read-only and may not be modified. The MC92603 only supports 1000BASE-X, full-duplex operation. Therefore, bit 15 is forced to a one and bits 14–12 are forced to zeros.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	1000BASE-X Full-Duplex	1000BASE-X Half-Duplex	1000BASE-T Full-Duplex	1000BASE-T Half-Duplex	Reserved											
W																
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-7. Extended Status Register (MDIO RA 15)

4.2.9 MDIO RA 16 (Vendor Specific)—Permanent Configuration Control Register

MDIO RA 16 is vendor specific and contains the MC92603 permanent configuration control register. These bits are initially loaded from the states of the corresponding configuration input pins. They may be modified through the MDIO interface, but if they are written through this interface, the logic within the MC92603 is reset, and normal operations will be interrupted until individual channels are resynchronized. Figure 4-8 shows the content of register 16.

	15	14	13	12	11	10	9	8
R W	xmit_ref_a	recv_ref_a	tbie	bsync	compat	rcce	repe	wsync1
Reset	XMIT_REF_A	RECV_REF_A	TBIE	BSYNC	COMPAT	RCCE	REPE	WSYNC1

	7	6	5	4	3	2	1	0
R W	wsync0	jpack	adie	tst_1	tst_0	lboe	use_short_ an_timer	ddr
Reset	WSYNC0	JPACK	ADIE	TST_1	TST_0	LBOE	0	DDR

Figure 4-8. Permanent Configuration Control Register (MDIO RA 16)

NOTE

Only one copy of this register exists within GEt. It may be accessed through any of the four channels, but if modified it affects operation of all four channels.

Table 4-6 lists the corresponding field descriptions for the permanent configuration register.

Table 4-6. Permanent Configuration Control Register Field Descriptions

Bits	Name	Description[1]
15	xmit_ref_a_reg	Initialized to the value on the XMIT_REF_A input. If set, indicates that all transmit data into the transmitter is synchronous with channel A's transmit clock (XMIT_A_CLK). (R/W)
14	recv_ref_a_reg	Initialized to the value on the RECV_REF_A input. If set, indicates that all receive data out of the receiver is synchronous with channel A's recovered clock (RECV_A_RCLK). (R/W)
13	tbie_reg	Initialized to the value on the TBIE input. If set, indicates that data into the transmitter and out of the receiver is to be treated as ten-bit coded data. (R/W)
12	bsync_reg	Initialized to the value on the BSYNC input. If set, indicates that data out of the receiver is to be byte aligned using COMMA code groups. (R/W)
11	compat_reg	Initialized to the value on the COMPAT input. If set, indicates that if context sensitive, data will be dropped or repeated to prevent overrun/underrun. See Chapter 5, "System Design Considerations," for an explanation. (R/W)

Table 4-6. Permanent Configuration Control Register Field Descriptions (continued)

Bits	Name	Description[1]
10	rcce_reg	Initialized to the value on the RCCE input. If set, indicates that the received data clock frequency should be at the 'recovered' clock rate. If reset, then receive data frequency is derived from the 'reference' clock. See Section 3.6.1, "Recovered Clock Timing Mode (RCCE = High)" and Section 3.6.2, "Reference Clock Timing Mode (RCCE = Low)," for an explanation. (R/W)
9	repe_reg	Initialized to the value on the REPE input. If set, indicates that received data is to be wrapped around to transmitter to configure as a 'repeater.' This is for test purposes only. For details, see Section 5.5, "Repeater Mode," and the explanation in this Chapter 4, "Management Interface (MDIO)." (R/W)
8	wsync1_regl	Initialized to the value on the WSYNC1 input. If set, indicates that received data for all four channels is to be aligned into one 32-bit word output. See Section 3.5.3, "Word Synchronization," for an explanation. (R/W)
7	wsync0_reg	Initialized to the value on the WSYNC0 input. If set, specifies that a 'disparity style word sync event' is to be used. See Section 3.5.3, "Word Synchronization," for details. (R/W)
6	jpack_reg	Initialized to the value on the jpack input. If set, allows 'jumbo' packets of data to be received (lengthens the receive FIFO). See Section 3.7.2.4, "Data Context," for details. (R/W)
5	adie_reg	Initialized to the value on the ADIE input. If receivers are set to 'reference clock mode' (rcce_reg = 0), setting, adie_reg allows code groups to be inserted/deleted to prevent overrun/underrun. See Section 3.6.2, "Reference Clock Timing Mode (RCCE = Low)," for details. (R/W)
4	tst_1	Initialized to the value on the TST_1 input. Used together with tst_0_reg to configure various test modes for the MC92603. (R/W)
3	tst_0	Initialized to the value on the TST_0 input. Used together with tst_1_reg to configure various test modes for the MC92603. (R/W)
2	lboe	Initialized to the value on the LBOE input. If set, indicates that if this channel's transmit data is to be digitally looped back (XCVR_*x*_LBE = 1), that the corresponding transmit link (XLINK_*x*_P and XLINK_*x*_N) will be active. If LBOE is low, the link will be quiescent during loopback. (R/W)
1	use_short_ an_timer	Initialized to zero. May be set through the MDIO interface only. If set it causes the auto negotiation timer to rollover after 2 microseconds instead of the usual 10 milliseconds. Note that this is for use during test only. (R/W)
0	ddr	Initialized to the value on the DDR input. If set, causes the MC92603 to use a DDR interface. See Section 2.5.1.2, "Ethernet Data Transmission Process" and Section 3.7.1.3, "Double Data Rate Operation—RGMI and RTBI." (R/W)

[1] R/W = read and write.

4.2.10 MDIO RA 17 (Vendor Specific)—Channel Configuration and Status Register

MDIO RA 17 contains the MC92603 channel configuration and status register. These bits are initially loaded on power up from the corresponding states of the external MC92603 configuration input pins. They may be modified through the MDIO interface. It is not necessary to reset the device logic if these bits are modified. Figure 4-9 shows the content of register 17.

	15	14	13	12	11	10	9	8
R	m_xcvr_ disable	i_xcvr_ disable	overrun	underrun	an_mode	recv_clk_cent	broadcast_ mode	xcvr_*x*_rsel
W								
Reset	0	XCVR_*x*_ DISABLE	0	0	0	RECV_CLK_ CENT	BROADCAST	XCVR_*x*_ RSEL

	7	6	5	4	3	2	1	0
R	Receiver Error Counter							
W								
Reset	0	0	0	0	0	0	0	0

Figure 4-9. Channel Configuration and Status Register (MDIO RA 17)

Table 4-7 lists the corresponding field descriptions for the channel configuration and status register.

Table 4-7. Channel Configuration and Status Register Field Descriptions

Bits	Name	Description[1]
15	*m*_xcvr_disable	Initialized to zero. May be written through the MDIO interface. A software disable, when set indicates that channel is to be disabled to reduce power. The channel is disabled if either bit 15 or 14 are set. (R/W)
14	i_xcvr_*x*_disable	Contains the value of the XCVR_*x*_DISABLE input. (R)
13	overrun	Bit 13 is initialized to zero and then is set to one only if this channel ‘overruns’ due to clock mismatch between the transmitter and receiver. Once set this bit is ‘sticky.’ That is, it remains set until register 17 is read through the MDIO interface. This bit may not be written through the MDIO interface. (R, LH, SC)
12	underrun	Bit 12 is initialized to zero and then is set to one only if this channel ‘underrun’ due to clock mismatch between the transmitter and receiver. Once set this bit is ‘sticky.’ That is, it remains set until register 17 is read through the MDIO interface. This bit may not be written through the MDIO interface. (R, LH, SC)
11	an_mode	Initialized to zero. This bit is set whenever this channel’s transmitter is in the auto-negotiation mode. This bit may not be written through the MDIO interface. (R)
10	recv_clk_cent	Initialized to RECV_CLK_CENT input. May be written through the MDIO interface. If set, indicates that data out of the receiver is centered relative to the RECV_*x*_RCLK output. (R/W)
9	broadcast	Initialized to BROADCAST input if in redundant mode (ENAB_RED input is high). May be written through the MDIO interface if in redundant mode. If set indicates that data will be transmitted over both of the transmit links. Only applicable to Channel A and B. (R/W)

Table 4-7. Channel Configuration and Status Register Field Descriptions (continued)

Bits	Name	Description[1]
8	xcvr_*x*_rsel	Initialized to XCVR_*x*_RSEL input if in redundant mode (ENAB_RED input is high). May be written through the MDIO interface. If set indicates that data will be transmitted/received over the secondary (redundant) links. Only applicable to Channel A and B. (R/W)
7–0	recv_error_ctr	Initialized to zero. This 8-bit counter is incremented whenever this channel's receiver detects a code error or disparity error. This counter is cleared when read through the MDIO interface. This counter cannot be loaded (other than cleared) through the MDIO interface. If counter reaches maximum value (0xFF) it will not roll over to zero; instead it will stay at this value until read. This register is to give a quick (although not precisely accurate) reading on bit error rate. Implementation limitations may cause some errors not to be counted. (R, SC)

[1] LH = Latched high, R = read only, R/W = read and write, and SC = self-clearing.

4.2.11 MDIO RA 18 (Vendor Specific)—BERT Error Counter Register

The MDIO RA 18, shown in Figure 4-10, contains the MC92603 BERT error counter register. These bits are initially cleared to all zeros. They may be read through the MDIO interface. They are updated from the appropriate channel's BERT error counter when running any of the BERT tests.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved								BERT Error Counter Value							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-10. BERT Error Counter Register (MDIO RA 18)

Chapter 5
System Design Considerations

This chapter consists of the following sections:

This chapter describes general system considerations for the MC92603 Quad Gigabit Ethernet transceiver, including the following:

- Device startup
- Initialization and proper use of the configuration and control signals
- Reference clock configuration
- General recommendations

5.1 Reference Clock Configuration

The MC92603 provides the option of either a differential or single-ended source for the reference clock input. The frequency of the clock signal applied to these inputs along with the settings on the configuration inputs determine the speed at which the serial links operate. Also, the legal ranges of reference clock frequencies vary depending on the state of the half-speed enable, HSE, input. Table 5-1 shows the allowable ranges for each configuration.

Table 5-1. Legal Reference Clock Frequency Ranges

HSE	Reference Frequency Min (MHz)	Reference Frequency Max (MHz)	Link Transfer Rate (Gigabaud)
Low	95.00	135.0	0.95–1.35
High	47.50	67.50	0.475–0.675

The internal reference clock may be driven by either a 3.3-V (LVTTL) input (TTL_REF_CLK) or by a pair of LVPECL differential inputs (REF_CLK_P and REF_CLK_N). If the USE_DIFF_CLOCK input is high, the LVPECL differential inputs, REF_CLK_P and REF_CLK_N, are used as the clock source. If USE_DIFF_CLOCK is low, the TTL_REF_CLK input is used as the clock source.

The differential reference clock inputs, REF_CLK_P/N, may also be driven by a single-ended source. The REF_CLK_N input must be set at V_{REF} = 1.25 V for a single-ended operation of REF_CLK_P and must be connected to its own reference voltage circuit.

When using the differential LVPECL inputs, the unused input, TTL_REF_CLK, shall be terminated low. When using the single-ended TTL input, the differential LVPECL reference clock inputs shall be terminated low.

5.2 Startup

The MC92603 begins a startup sequence on application of the reference clock input to the device. This is considered a cold startup. The cold startup sequence is as follows:

1. PLL startup
2. Receiver initialization and byte alignment
3. Word alignment (if enabled)
4. Run

The expected duration of each step in the startup sequence is shown in Table 5-2. A cold startup can be initiated at any time by negating $\overline{\text{RESET}}$ low. It is recommended that $\overline{\text{RESET}}$ be low at initial startup, but, it is not strictly required.

Table 5-2. Startup Sequence Step Duration

Startup Step	Typical Duration (in Bit Times)	Notes
PLL startup	20480 + 25 μs	
Receiver initialization	300	WSYNC1 and WSYNC0 = low
Word alignment	160	WSYNC1 or WSYNC0 = high

5.3 Standby Mode

Standby mode puts the MC92603 into a low power, inactive state. When STNDBY is asserted high, the device will force all transmitter link outputs to their disabled state as defined in Section 2.3.1, “Transmit Driver Operation,” and disables all internal clocking. An important feature of standby mode is that the internal PLL is not disabled. It remains operating and locked to the reference clock. This greatly reduces the time needed to recover from standby mode to run mode, as only the receiver initialization and word alignment startup steps are required.

5.4 Receiver Interface Clock Centering

All interface output drivers are internally source terminated with 50 Ω. Therefore, no external source terminations are required.

The receiver interface also has the option of having the output data source-aligned or source-centered with the respective channel RECV_x_CLK. If source-aligned, then the considerations for pcb design must include lengthening the clock trace to meet interface setup time requirements. However, the suggested method would be to use the source-centered option to maximize the setup and hold times, keeping the clock and data traces the same length. This applies for all modes of operation (backplane or Ethernet compatibility and normal or reduced interface modes). For more information, see Section 3.6, "Receiver Interface Timing Modes," and the specifications in Section 7.3.2, "Receiver Interface Timing."

5.5 Repeater Mode

The MC92603 may be configured into a two-link receive-transmit repeater by setting the repeater mode enable, REPE, signal high. In repeater mode, data received on link A's receiver is forwarded to link A's transmitter and link B's receiver to link B's transmitter. The configuration inputs may be used to control how the repeater handles the data as it passes through the repeater. Certain configurations are more effective than others for various applications. The transmitter at the source, the receiver at the destination, and the repeater must have compatible configurations to ensure proper operation. The following sections describe how each configuration control affects the repeater operation.

NOTE

The primary purpose of this mode is to facilitate bit error rate testing with the test data driven into GEt through the receiver serial links and then is sent back to the BERT tester through the transmitter serial links.

This mode does not attempt to meet the standard for Ethernet repeaters as defined in Clause 41 of IEEE Std. 802.3-2002 [4].

5.5.1 Ten-Bit Interface Mode

When the device is in 10-bit interface mode (TBIE = high), the internal 8B/10B encoder and decoder are bypassed and the 10-bit data received is forwarded directly to the transmitter. Running disparity is assumed correct and is not checked.

When byte interface mode is enabled (TBIE = low), received data is passed through the 8B/10B decoder where it is converted into its 8-bit data or a control byte. Running disparity and code validity are checked and reported with the received byte at the receiver interface, as described in Section 3.8.1, "Byte Mode (Uncoded Data)." The decoded byte is re-coded by the transmitter's 8B/10B encoder for transmission.

5.5.2 Byte Alignment Mode

Byte alignment mode must be enabled (BSYNC = high) for repeater mode.

When establishing byte alignment for the link through the repeater, the byte alignment sequence must be repeated twice:

- Once for the repeater
- Once for the destination's receiver

At least eight IDLE code groups must be transmitted, four for the repeater's receiver alignment and four for the destination's receiver alignment.

5.5.3 Word Synchronization Mode

Word synchronization may be used in repeater mode. This allows the incoming bytes to be synchronized into their corresponding words, removing cable skew from the transmission source and re-establishing synchronization.

Similar to byte alignment, the word synchronization sequence must be repeated twice, once for the repeater and once for destination's receiver. A word synchronization event must be transmitted followed by a second word synchronization event to enable the entire link to establish word synchronization. Byte alignment must be established, as described in Section 5.5.2, "Byte Alignment Mode," prior to word synchronization.

5.5.4 Recovered Clock Mode

The MC92603's four transmitters are timed exclusively to the reference clock domain; therefore, the recovered clock mode cannot be used in repeater mode. The setting on the recovered clock enable input, RCCE, is ignored when in repeater mode, and all data is timed to the reference clock.

5.5.5 Add/Drop Idle Mode

Repeater mode is timed exclusively to the reference clock domain as stated above. A frequency offset between the source transmitter and the repeater will cause the repeater's receiver to eventually overrun/underrun. To ensure that overrun/underrun does not cause data to be lost, ADIE must be high. The repeater repeats or drops data from the data stream to maintain alignment to the reference clock (see Section 3.6.2, "Reference Clock Timing Mode (RCCE = Low)," for specifics).

5.5.6 Half-Speed Mode

Half-speed mode simply affects the frequency of the reference clock that must be provided and the timing of the receiver interface. This mode is supported in the repeater mode.

5.6 Configuration and Control Signals

The MC92603 has many configuration and control signals that are asynchronous to all input clocks. Most of the signals affect the internal configuration state and must be set at power up. If the signal's state is changed after power up, some signals require that the device be reset by asserting $\overline{\text{RESET}}$ low and then releasing high. Other configuration signals are meant to be changed during normal operation and do not require a device reset. However, these signals may still affect device operation. Table 5-3 lists all of the MC92603 asynchronous configuration and control signals and describes the effect of changing their state after power up.

If MDIO is enabled, then the states may be modified via the MDIO interface. When MDIO_EN is asserted, the configuration states are loaded on reset as before, and may then be modified through the interface. The configuration states are read via registers 1, 16, and 17. If any of the hardwired configurations change when MDIO_EN is asserted, the device must be reset for the action to be initiated. For example, if MDIO_EN is high, changing the configuration input, XCVR_x_LBE, will be ignored until reset is asserted.

Table 5-3. Asynchronous Configuration and Control Signals

Signal Name	Description	Effect of Changed State
XCVR_*x*_DISABLE	Transceiver disable	Receiver must acquire new bit phase alignment; byte and word synchronization must be re-established.
XCVR_x_LBE	Transceiver loopback enable	Receiver must acquire new bit phase alignment; byte and word synchronization must be re-established.
DROP_SYNC	Drop synchronization	Receiver must re-establish byte and word synchronization.
XMIT_REF_A	Transmitter reference clock A select	Device must be reset
RECV_REF_A	Receiver reference clock A select	Device must be reset
TBIE	Ten-bit interface enable	Device must be reset
HSE	Half-speed enable	Device must be reset
BSYNC	Byte synchronization mode	Device must be reset
ADIE	Add/drop idle enable	Device must be reset
JPAK	Expand receiver FIFO to tolerate Jumbo packets	Device must be reset
COMPAT	Ethernet compatibility mode	Device must be reset
ENABLE_AN	Enable auto-negotiate	Device must be reset
RCCE	Recovered clock enable	Device must be reset
REPE	Repeater mode enable	Must be low and remain low during normal operation. Device must be reset if changed.
WSYNC1	Word synchronization enable	Device must be reset
WSYNC0	Word synchronization enable	Device must be reset

Table 5-3. Asynchronous Configuration and Control Signals (continued)

Signal Name	Description	Effect of Changed State
TST_0, TST_1	Test mode identifiers	Must be low and remain low during normal operation. Device must be reset if changed.
LBOE	Loopback output enable	Enable/disable transmit links during testing (LBOE = high). No recovery action necessary,
STNDBY	Puts PLL in standby mode	Receiver must re-establish byte and word synchronization
$\overline{\text{RESET}}$	System reset bar	Device is reset
ENABLE_RED	Enable redundant mode	Device must be reset

5.7 Power Supply Requirements

The recommended board for the MC92603 has a minimum of two solid planes of 1-ounce copper. One plane is to be used as a ground plane and the second plane is to be used for the 1.8-V supply. It is recommended that the board has its own 1.8- and 3.3-V regulators with less than 50-mV ripple.

5.8 Phase-Locked Loop (PLL) Power Supply Filtering

An analog power supply is required. The $PLLAV_{DD}$ signal provides power for the analog portions of the PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in Figure 5-1. For maximum effectiveness, the filter circuit is placed as close as possible to the $PLLAV_{DD}$ ball to ensure that it filters out as much noise as possible. The ground connection should be near the PLLAGND ball. The 0.01-µF capacitor is closest to the ball, followed by the 1-µF capacitor, and finally the 1-Ω resistor to V_{DD} on the 1.8-V power plane. The capacitors are connected from PLLAGND to the ground plane. Ceramic chip capacitors with the highest possible self-resonant frequency should be used. All traces should be kept short, wide, and direct.

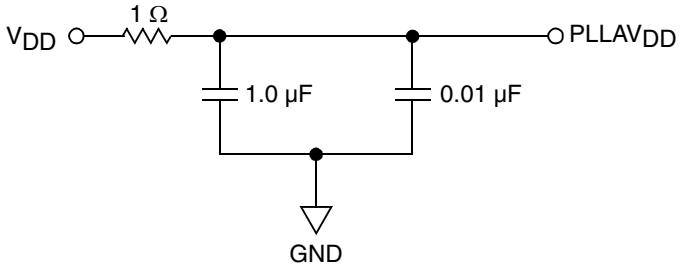


Figure 5-1. PLL Power Supply Filter Circuits

5.9 Power Supply Decoupling Recommendations

The MC92603 requires a clean, tightly regulated source of power to ensure low jitter on transmit, and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used, in order to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

First, the board should have about 10 × 10-nF SMT ceramic chip capacitors as close as possible to the 1.8-V (V_{DD} and XV_{DD}) balls of the device. The board should also have about 10 × 10 nF SMT ceramic chip capacitors as close as possible to the V_{DDQ} balls of the device. Where the board has blind vias, these capacitors should be placed directly below the MC92603 supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the MC92603, as close to the supply and ground connections as possible.

Second, there should be a 1-µF ceramic chip capacitor on each side of the MC92603 device. This should be done for both the 1.8-V supply and the V_{DDQ} supply.

Finally, there should be a 10-µF low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF low ESR SMT tantalum chip capacitor between the MC92603 device and the voltage regulator. This should be done for both the 1.8-V supply and the V_{DDQ} supply.

Chapter 6
Test Features

This chapter consists of the following sections:

- Section 6.1, “IEEE Std. 1149.1 Implementation”
- Section 6.2, “System Accessible Test Modes”
- Section 6.3, “BIST Sequence Test with Internal Digital Loopback Mode”

The MC92603 supports several test modes for built-in system test, BIST, and production testing. The MC92603 also has an IEEE Std. 1149.1 [3] compliant test access port and boundary scan architecture implementations. This chapter covers the JTAG implementation and the system accessible test modes.

6.1 IEEE Std. 1149.1 Implementation

This section describes the IEEE Std. 1149.1 compliant test access port and boundary scan architecture implementation in the MC92603.

6.1.1 Test Access Port (TAP) Interface Signals

Table 6-1 lists the interface signals for the TAP.

Table 6-1. TAP Interface Signals

Signal Name	Description	Function	Direction	Active State
TCK	Test clock	Test logic clock	Input	—
TMS	Test mode select	TAP mode control input	Input	—
TDI	Test data in	Serial test instruction/data input	Input	—
$\overline{\text{TRST}}$	Test reset bar	Asynchronous test controller reset	Input	Low
TDO	Test data out	Serial test instruction/data output	Output	—

NOTE

The TMS, TDI, and $\overline{\text{TRST}}$, have 100-KΩ pull-ups. If $\overline{\text{TRST}}$ is not held low during power up or does not receive an active low preset after power up, the test logic may assume an indeterminate state disabling some of the normal transceiver functions. It is recommended that $\overline{\text{TRST}}$ be terminated in one of the following ways:

- Drive $\overline{\text{TRST}}$ with a TAP controller that provides a reset after power up.
- Connect $\overline{\text{TRST}}$ to $\overline{\text{RESET}}$.
- Terminate $\overline{\text{TRST}}$ with a 1-KW resistor (or hardwire) to ground.

6.1.2 Instruction Register

Figure 6-1 shows the format for the instruction register.

Bit Position	3	2	1	0
Field	IR			
Capture-IR Value	0	0	0	1

Figure 6-1. Instruction Register

6.1.3 Instructions

Table 6-2 lists the public instructions provided in the implementation and their instruction codes.

Table 6-2. Tap Controller Public Instructions

Instruction	Code	Enabled Serial Test Data Path
BYPASS	1111	Bypass register
CLAMP	1100	Bypass register
EXTEST	0000	Boundary scan register
HIGHZ	1001	Bypass register
IDCODE	0001	ID register
SAMPLE	0010	Boundary scan register

Table 6-3 lists the private instruction codes that can be hazardous to the device operation if executed. The user should not execute these instructions.

Table 6-3. Tap Controller Private Instruction Codes

Instruction Code	Instruction Code
0011	1000
0100	1010
0101	1011
0110	1110
0111	—

6.1.4 Boundary Scan Register

A full description of the boundary scan register may be found in the boundary scan description language (BSDL) file provided by Freescale upon request.

6.1.5 Device Identification Register (0x0281E01D)

Figure 6-2 shows the format for the device identification register. All bits of the register are read-only.

	31			28	27													12	11										0
R	VERSION				PART NUMBER														MANUFACTURER ID										
W																													
Reset	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1

Figure 6-2. Device Identification Register

6.1.6 Performance

The performance and electrical properties of the TAP controller, boundary scan, and JTAG inputs and outputs, are described in Chapter 7, "Electrical Specifications and Characteristics."

6.2 System Accessible Test Modes

System accessible test modes are selected through the TST_0, TST_1, and XCVR_A_LBE signals. Table 6-4 shows test mode state selection.

Table 6-4. Test Mode State Selection

TST_1	TST_0	XCVR_A_LBE	Description
Low	Low	Low	Normal operation. No test mode enabled.
Low	Low	High[1]	Internal loopback system test mode
Low	High	Low	System BIST sequence—external loopback—no idles inserted
Low	High	High	System BIST sequence—external loopback—with idles inserted
High	Low	Low	System BIST sequence—internal loopback—with idles inserted
High	Low	High	Reserved
High	High	Low	Reserved
High	High	High	Reserved

[1] If TST_1 and TST_0 are both low, each channel is controlled by its own LBE (channel A = XCVR_A_LBE, channel B = XCVR_B_LBE, etc.). If either TST_1 or TST_0 is high, then XCVR_A_LBE is used to select BIST test modes for all channels, and XCVR_B_LBE, XCVR_C_LBE, and XCVR_D_LBE are ignored.

6.2.1 Loopback System Test

Each channel of MC92603 may be individually configured for digital loopback, where the transmitted data is looped back to its receiver independent of the receiver's link inputs. This is enabled by asserting XCVR_*x*_LBE (where '*x*' is channel A through D) high. The code groups transmitted are controlled by the normal transmitter controls. If the transceiver is working properly, the data/control code groups transmitted are received internally by the receiver. This allows system logic to use various data sequences to test the operation of the transceiver.

The loopback signals are electrically isolated from the XLINK_*x*_P and XLINK_*x*_N output signals. Therefore, if the outputs are externally shorted, or otherwise restricted, the loopback signals still function normally. When in loopback mode, the XLINK_*x*_P and XLINK_*x*_N output signals will continue to operate normally.

The receiver's link input signals, RLINK_*x*_P and RLINK_*x*_N, are electrically isolated during loopback mode, such that their state does not affect the loopback path.

LBOE controls the state of the XLINK_*x*_P/XLINK_*x*_N output signals during loopback testing. If LBOE is low, XLINK_*x*_P/XLINK_*x*_N are held to low and high, respectively. If LBOE is high, data is present on XLINK_*x*_P/XLINK_*x*_N.

6.2.2 BIST Sequence System Test with External Loopback Modes

The MC92603's transmitter has an integrated, 23rd order, pseudo-noise (PN) pattern generator. Stimulus from this generator may be used for system testing. The receiver, has a 23rd order signature analyzer that is synchronized to the incoming PN stream and may be used to count code group mismatch errors relative to the internal PN reference pattern.

This implementation of the 23-bit PN generator and analyzer uses the following polynomial:

$$f = 1 + x^5 + x^{23}$$

The total mismatch error count is reset to zero on entering BIST mode. The count is updated continuously while in BIST mode. The value of the count is presented on the receiver interface signals, RECV_*x*_7–RECV_*x*_0, which make up the 8-bit error count. The value of the count is sticky in that the count will not wrap to zero on overflow, but rather, stays at the maximum count value (11111111).

NOTE

An error counter is maintained in MDIO RA 18 for each specific channel in all BIST test modes. See Chapter 4, "Management Interface (MDIO)," for details.

The RECV_*x*_ERR, RECV_*x*_DV, and RECV_*x*_COMMA signals, as interpreted and shown in Table 6-5, have special meaning in this test mode. They report the status of the receiver and PN analysis logic.

Table 6-5. BIST Error Codes

RECV_*x*_ERR	RECV_*x*_DV	RECV_*x*_COMMA	Description
Low	Low	Don't care	Not byte/word sync. The receiver is in start-up or has lost byte alignment and is searching for alignment.
Low	High	Low	BIST running. No PN mismatch this code group.
Low	High	High	BIST running. This code group is a COMMA code group.
High	Low	Don't care	Receiver byte/word synchronized. PN analyzer is not locked.
High	High	Don't care	BIST running. PN mismatch error for this code group.

The BIST sequence makes use of the 8B/10B encoder/decoder. Therefore, this test mode overrides the setting on the TBIE signal and forces byte interface mode. Additionally, the BIST sequence requires that a normal byte alignment mode be used. The setting of BSYNC is overridden, forcing the device into the byte aligned mode, which forces BSYNC high internally.

BIST is run at the speed indicated by the frequency of the reference clock and by the speed range selected by half-speed mode (HSE). Word sync mode is supported during BIST testing, however, only the 4-IDLEs/Non-IDLE alignment mode is supported (WSYNC1 = low and WSYNC0 = high).

The BIST sequence is as follows:

1. Enter test mode by setting the test mode inputs as described in Table 6-4.
2. If COMPAT is low, transmit 4096 IDLEs (K28.5 characters).
   If COMPAT is high, an auto-negotiation sequence will occur.
3. Transmit an 8B/10B encoded PN sequence to the receiver as described above.

The transmitter will automatically go through sequences 2 and 3 on entering this test mode. When testing is complete, the device will need to be reset before normal operation can resume.

If IDLEs are to be inserted (TST_1 = low, TST_0 = high, XCVR_A_LBE = high), then IDLEs (K28.5 code group) are inserted every 2048 code groups during sequence 3.

If COMPAT is high, /I1/I2/ code groups will be inserted instead of the IDLE (K28.5) code group.

6.3 BIST Sequence Test with Internal Digital Loopback Mode

This test mode is identical to the system BIST sequence test with external loopback mode described above, except loopback is performed internally to GEt.

NOTE

In this mode, the configuration input LBOE controls whether serial data is sent on transmit link outputs (XLINK_*x*_P and XLINK_*x*_N). If LBOE is low, the link is quiescent; if LBOE is high, data is transmitted on the link).

Chapter 7
Electrical Specifications and Characteristics

This chapter provides the MC92603 electrical specifications and characteristics. This chapter consists of the following sections:

7.1 General Characteristics

This section provides the general parameters, absolute maximum ratings, and recommended operating conditions for the MC92603.

7.1.1 General Parameters

A summary of the general parameters for the MC92603 are as follows:

Package	256 MAPBGA, 17 x 17 mm body size, 1 mm ball pitch
Core power supply	1.8 V $\pm$ 0.15 V DC
I/O power supply	3.3 V $\pm$ 0.3 V DC or 2.5 V $\pm$ 0.2 V DC
Link I/O power supply	1.8 V $\pm$ 0.15 V DC

7.1.2 Absolute Maximum Rating

The MC92603 absolute maximum ratings are described in Table 7-1.

Table 7-1. Absolute Maximum Ratings

Characteristics[1]	Symbol	Min	Max	Unit
Core supply voltage	V_{DD}	–0.3	2.2	V
PLL supply voltage	AV_{DD}	–0.3	2.2	V
LVCMOS/TTL I/O supply voltage	$V_{DD}Q$	–0.3	4.0	V
Link I/O supply voltage	XV_{DD}	–0.3	2.2	V
LVCMOS/TTL input voltage	V_{in}	–0.3	$V_{DD}Q$ + 0.3	V
Link input voltage	V_{in}	–0.3	XV_{DD} + 0.3	V
Storage temperature range	T_{stg}	–55	150	°C
ESD tolerance	HBM	2000	—	V
	MM	200	—	V

1 Functional and tested operating conditions are given in Table 7-2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums are not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

7.1.3 Recommended Operating Conditions

This section describes the recommended operating conditions for the MC92603 as provided in Table 7-2.

Table 7-2. Recommended Operating Conditions

Characteristic[1,2]	Symbol	Min	Max	Unit
Core supply voltage	V_{DD}	1.65	1.95	V
PLL supply voltage	AV_{DD}	1.65	1.95	V
LVCMOS/TTL I/O supply voltage (3.3-V operation)	$V_{DD}Q$	3.0	3.6	V
LVCMOS/TTL I/O supply voltage (2.5-V operation)	$V_{DD}Q$	2.3	2.7	V
Link I/O supply voltage	XV_{DD}	1.65	1.95	V
LVCMOS/TTL input voltage	V_{in}	0	$V_{DD}Q$	V
Link input voltage	V_{in}	0	XV_{DD}	V
Junction temperature	T_j	–40	105	°C
Ambient temperature[3]	T_a	—	—	°C

1 These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

2 Recommended supply power-up order is V_{DD}, AV_{DD}, V_{DDQ}, XV_{DD}, however, any order is acceptable as long as maximum ratings are not exceeded.

3 Operating ambient temperature is dependent on proper thermal management to meet operating junction temperature.

7.2 DC Electrical Specifications

This section describes the MC92603 DC electrical characteristics as provided in Table 7-3.

Table 7-3. DC Electrical Specifications

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Core supply current [2]	I_{DD}	—	220	300	mA
PLL supply current [2]	AI_{DD}	—	8	10	mA
LVCMOS/TTL I/O supply current [2]	$I_{DD}Q$	—	55	75	mA
Link I/O supply current [2]	XI_{DD}	—	110	155	mA
Total power dissipation [3]	P_D	—	860	1150	mW
LVCMOS/TTL input high voltage	V_{IH}	1.7	—	$V_{DD}Q$ + 0.3	V
LVCMOS/TTL input low voltage	V_{IL}	–0.3	—	0.7	V
LVCMOS/TTL input leakage current, V_{in} = V_{DDQ}	I_{IH}	—	—	±10	μA
LVCMOS/TTL input leakage current, V_{in} = GND	I_{IL}	—	—	±10	μA
LVCMOS/TTL output high voltage, I_{OH} = –7.6 mA	V_{OH}	1.76	—	—	V
LVCMOS/TTL output low voltage, I_{OL} = 7.6 mA	V_{OL}	—	—	0.54	V
LVCMOS/TTL output high voltage, I_{OH} = –2 mA	V_{OH}	2.0	—	—	V
LVCMOS/TTL output low voltage, I_{OL} = 2mA	V_{OL}	—	—	0.4	V
LVCMOS/TTL input capacitance	C_{in}	—	—	10	pF
LVCMOS/TTL output impedance, Vout = V_{DDQ}/2	R_{out}	—	50	—	W
LVPECL AC differential input voltage	V_{PKPK}	0.4	—	1.3	V
LVPECL differential cross point voltage	V_{CMR}	1.25	—	$V_{DD}Q$ – 0.3	V
LVPECL input current	I_{IN}	—	—	±100	μA
Link common mode input impedance	R_{cm}	2	—	4	KΩ
Link differential input impedance (MEDIA = low/high)	R_{diff}	85/127.5	—	130/195	W
Link common mode input level[4]	V_{cm}	0.725	—	1.225	V
Link differential input amplitude	ΔV_{in}	0.4	—	3.2	V_{p-p}
Link input capacitance	C_{in}	—	—	3	pF
Link common mode output level	V_{cm}	0.725	0.9	1.075	V
Link differential output amplitude, (100/150Ω diff load, MEDIA = low/high)	ΔV_{out}	1.3	—	2.2	V_{p-p}
Link differential output impedance (MEDIA = low/high)	R_{out}	—	100/150	—	W

1 Unless otherwise noted: V_{DD} = AV_{DD} = V_{DD} = 1.8 ± 0.15 V DC, $V_{DD}Q$ = 3.3 ± 0.3 V DC, GND = 0 V DC, –40° ≤ T_j ≤ 105° C.

2 Maximum currents at V_{DD} = AV_{DD} = XV_{DD} = 1.95 V DC, V_{DDQ} = 3.6 V DC, all links operating at full-speed. Typicals are with nominal supply voltages.

3 Typical P_D (mWatts) = A + Bn + Cnf + Df; where n = number of active channels and f = reference frequency in MHz. Note: A, B, C and D are to be determined (TBD).

4 Subject to absolute voltage on link input pin remaining in recommended range per Table 7-2.

7.3 AC Electrical Characteristics

The figures and tables in the following sections describe the AC electrical characteristics of MC92603. All specifications stated are for T_j = –40° to 105°C, $V_{DD} = AV_{DD} = XV_{DD}$ = 1.65 to 1.95 V, V_{DDQ} = 3.0 to 3.6 V

7.3.1 Transmitter Interface Timing

The transmitter data interface may be configured in any of eight different application modes as described in Section 2.2, "Transmitter Interface Signals," and Table 2-2. The 8- and 10-bit interface mode timing is non-double data rate (non-DDR); the input data is sampled and stored on the rising edge of the transmit interface clock XMIT_*x*_CLK.

When operating in the reduced 4- or 5-bit backplane, or RGMII/RTBI Ethernet modes, the interface is double data rate (DDR) and the data is sampled and stored on both the rising and falling edges of the transmit interface clock XMIT_*x*_CLK.

The following two sections show the timing diagrams and specifications for the transmitter in the non-DDR and DDR configurations.

7.3.1.1 Transmitter Interface, Non-DDR Timing

Figure 7-1 provides the transmitter interface non-DDR interface timing diagram.

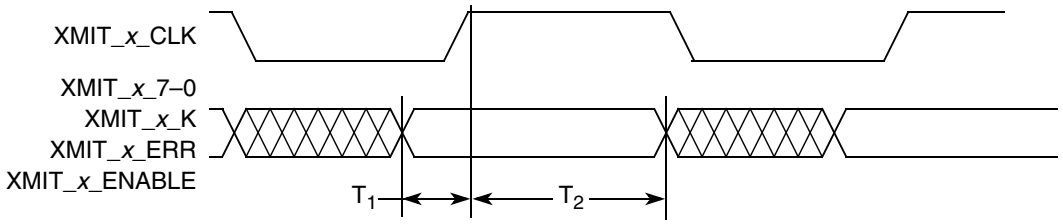


Figure 7-1. Transmitter Interface, Non-DDR Timing Diagram

Table 7-4 provides the transmitter non-DDR timing specifications for the MC92603 as defined in Figure 7-1.

Table 7-4. Transmitter Non-DDR Timing Specification

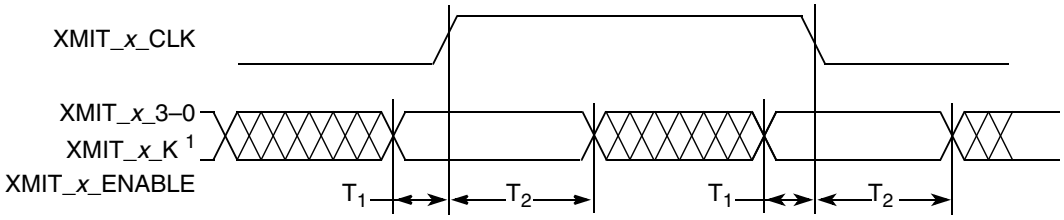
Symbol	Characteristic	Min	Max	Unit	Application Mode
T_1	Setup time prior to rising edge of XMIT_*x*_CLK	1.000	—	ns	All modes
T_2	Hold time after rising edge of XMIT_*x*_CLK	0.0[1]	—	ns	GMII or TBI
		0.200 [1]	—	ns	Backplane modes
		0.600[2]	—	ns	All modes
Φ_{drift}	Phase drift between XMIT_*x*_CLK and REF_CLK	–180	180	degrees	All modes

1 Synchronous to channel's transmit interface clock; XMIT_REF_A = low.

2 Synchronous to XMIT_A_CLK; XMIT_REF_A = high.

7.3.1.2 Transmitter Interface, DDR Timing

Figure 7-2 provides the transmitter interface DDR interface timing diagram.



1 Used only when transmitting uncoded data in backplane modes.

Figure 7-2. Transmitter Interface, DDR Timing Diagram

Table 7-5 provides the transmitter DDR timing specifications for the MC92603 as defined in Figure 7-2.

Table 7-5. Transmitter DDR Timing Specifications

Symbol	Characteristic	Min	Max	Unit	Application Mode
T_1	Setup time prior to rising/falling edge of XMIT_*x*_CLK	1.000	—	ns	All DDR modes
T_2	Hold time after rising/falling edge of XMIT_*x*_CLK	0.000[1,2]	—	ns	RGMII or RTBI
		0.200 [1]	—	ns	Backplane DDR modes
		0.600 [2]	—	ns	
Φ_{drift}	Phase drift between XMIT_*x*_CLK and REF_CLK	–180	180	degrees	All modes

1 Synchronous to channel's transmit interface clock; XMIT_REF_A = low.

2 Synchronous to XMIT_A_CLK; XMIT_REF_A = high.

7.3.2 Receiver Interface Timing

The data output timing at the receiver interface may be single data rate (non-DDR) or double data rate (DDR) as described in Section 3.4, "Receiver Interface Configuration." Additionally, the valid data is sourced simultaneously with, or centered on, the RECV_*x*_CLK output, depending on the state of the control signal, RECV_CLK_CENT.

When the control signal RECV_CLK_CENT = high, the data is centered about the receiver clock edge. When RECV_CLK_CENT = low, the receiver clock edge is aligned (co-incident) with the data. See Section 3.6, "Receiver Interface Timing Modes," for more on receiver interface timing.

Table 7-6 shows the receiver clock cycle time and the target or typical offset of the clock edge with respect to the data depending on the device application configuration. Note that the complement of the receiver clock, RECV_*x*_RCLK_B, is only valid and available in TBI and RTBI Ethernet compliant applications modes.

Table 7-6 also lists references to timing figures in the following receiver interface timing sections.

Table 7-6. Target Receiver Clock Offset Relative to Data

Application Mode	DDR	TBIE and COMPAT = High	HSE	Receiver Clock Cycle Time[1] (ns)	RECV_*x*_ RCLK	RECV_*x*_ RCLK_B	Clock Offset to Data (ns)	Reference Figure No.
GMII or 8-/10-bit backplane	Low	False	Low	8	Valid	Low	4	7-3
	Low	False	High	16	Valid	Low	8	7-3
Ethernet TBI	Low	True	Low	16	Valid	Valid	4	7-4
	Low	True	High	32	Valid	Valid	8	7-4
RGMII or 4-/5-bit backplane	High	False	Low	8	Valid	Low	2	7-5
	High	False	High	16	Valid	Low	4	7-5
Ethernet RTBI	High	True	Low	8	Valid	Valid	2	7-6
	High	True	High	16	Valid	Valid	4	7-6

[1] Assumes 125-MHz reference clock if HSE is disabled and 62.5-MHz reference clock if HSE is enabled.

7.3.2.1 Receiver Interface, Non-DDR Timing

The following sections provide the receiver, non-DDR timing specifications for the MC92603.

7.3.2.1.1 Receiver, Non-DDR Clock Timing (All Modes Except Ethernet TBI Modes)

Figure 7-3 provides the receiver interface, non-DDR timing diagram when TBIE is negated low or COMPAT is negated low.

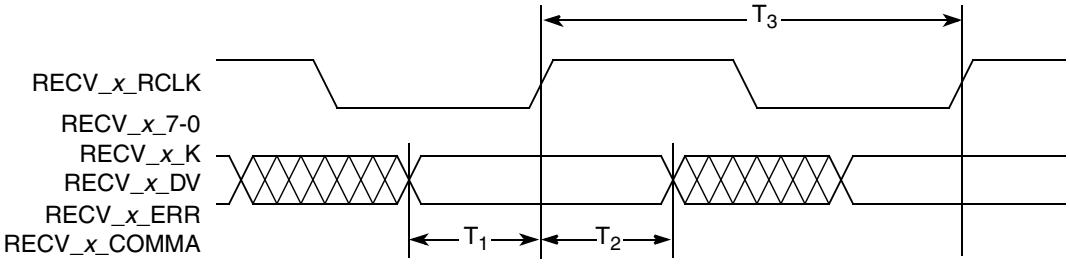


Figure 7-3. Receiver, Non-DDR Timing Diagram (TBIE = Low or COMPAT = Low)

Table 7-7 provides the receiver, non-DDR timing specifications when TBIE is negated low or COMPAT is negated low.

Table 7-7. Receiver, Non-DDR Timing Specifications (TBIE = Low or COMPAT = Low)

Symbol	Characteristic [1]	Aligned Clock		Centered Clock		Unit	Note
		Min	Max	Min	Max		
T_1	Output valid time before rising edge of RECV_x_RCLK	–0.500	0.500	3.500	—	ns	2
		–1.000	1.000	7.500	—	ns	3
T_2	Output valid time after rising edge of RECV_x_RCLK	7.000	—	3.500	—	ns	2
		15.000	—	7.500	—	ns	3
T_3	RECV_x_RCLK cycle time	7.800	8.200	7.800	8.200	ns	2
		15.800	16.200	15.800	16.200	ns	3

1 10 pF output load.

2 Full-speed, HSE = low.

3 Half-speed, HSE = high.

7.3.2.1.2 Receiver Interface, Non-DDR Clock Timing (Ethernet TBI Mode)

Figure 7-4 provides the receiver interface, non-DDR timing diagram when TBIE is asserted high and COMPAT is asserted high.

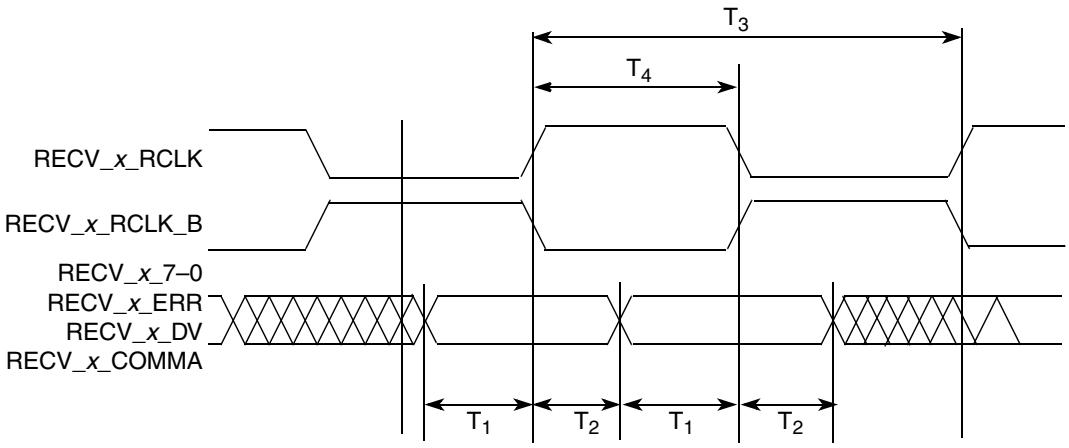


Figure 7-4. Receiver, Non-DDR Timing Diagram (TBIE = High and COMPAT = High)

Table 7-8 provides the receiver, non-DDR timing specifications when TBIE is asserted high and COMPAT is asserted high.

Table 7-8. Receiver, Non-DDR Timing Specifications (TBIE = High and COMPAT = High)

Symbol	Characteristic [1]	Aligned Clock		Centered Clock		Unit	Note
		Min	Max	Min	Max		
T1	Output valid time before rising edge of RECV_x_RCLK or RECV_x_RCLK_B	–0.500	0.500	3.500	—	ns	2
		–1.000	1.000	7.500	—	ns	3
T2	Output valid time after rising edge of RECV_x_RCLK or RECV_x_RCLK_B	7.000	—	3.500	—	ns	2
		15.000	—	7.500	—	ns	3
T3	RECV_x_RCLK or RECV_x_RCLK_B cycle time	15.80	16.20	15.800	—	ns	2
		31.80	32.20	31.800	—	ns	3
T4	Rising edge of RECV_x_RCLK to rising edge of RECV_x_RCLK_B	7.80	8.20	7.800	8.200	ns	2
		15.80	16.20	15.800	16.200	ns	3

1 10 pF output load.

2 Full-speed, HSE = low.

3 Half-speed, HSE = high.

7.3.2.2 Receiver Interface, DDR Timing

The following sections provides the receiver, DDR timing specifications for the MC92603.

7.3.2.2.1 Receiver, DDR Clock Timing (All Modes Except Ethernet RTBI Modes)

Figure 7-5 provides the receiver interface DDR timing diagram when TBIE is negated low or COMPAT is negated low.

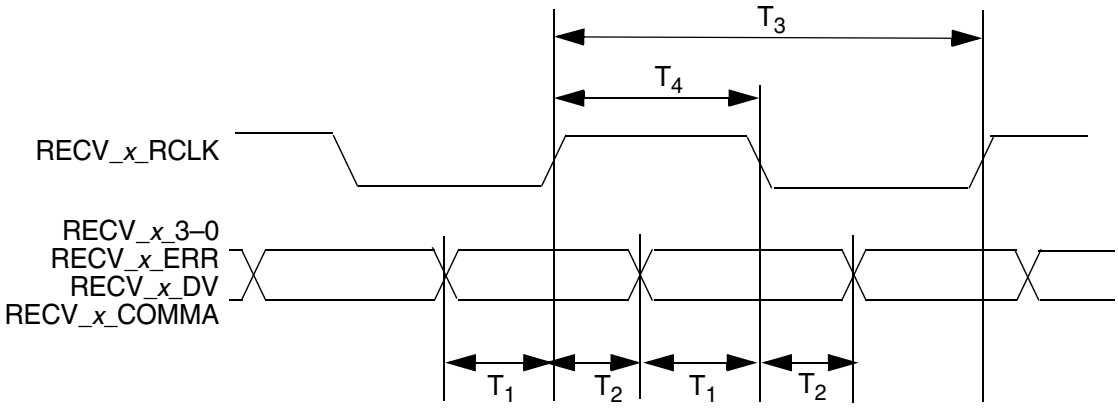


Figure 7-5. Receiver, DDR Timing Diagram (TBIE = Low or COMPAT = Low)

Table 7-9 provides the receiver, DDR timing specifications when TBIE is negated low or COMPAT is negated low.

Table 7-9. Receiver, DDR Timing Specification (TBIE = Low or COMPAT = Low)

Symbol	Characteristic [1]	Aligned Clock		Centered Clock		Unit	Note
		Min	Max	Min	Max		
T_1	Output valid time before rising/falling edge of RECV_x_RCLK	–0.500	0.500	1.440	—	ns	2
		–1.000	1.000	3.440	—	ns	3
T_2	Output valid time after rising/falling edge of RECV_x_RCLK	3.000	—	1.420	—	ns	2
		7.000	—	3.500	—	ns	3
T_3	RECV_x_RCLK cycle time	7.800	8.200	7.800	8.200	ns	2
		15.800	16.200	15.800	16.200	ns	3
T_4	RECV_x_RCLK half-cycle time	3.800	4.200	3.800	4.200	ns	2
		7.800	8.200	7.800	8.200	ns	3

1 10 pF output load.

2 Full speed, HSE = low.

3 Half speed, HSE = high.

7.3.2.2.2 Receiver, DDR Clock Timing (Ethernet RTBI Mode)

Figure 7-6 provides the receiver interface, DDR timing diagram when TBIE is asserted high and COMPAT is asserted high.

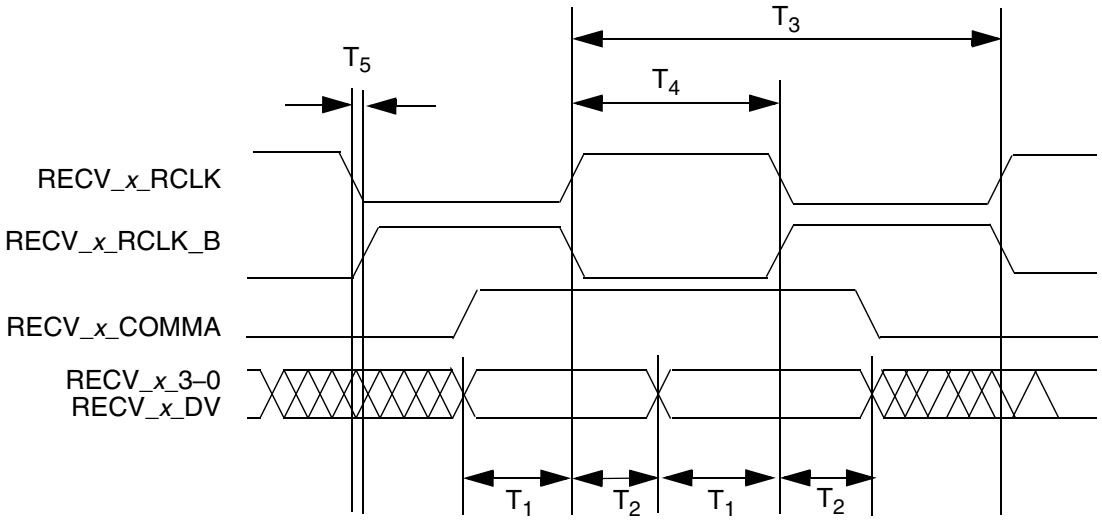


Figure 7-6. Receiver, DDR Timing Diagram (TBIE = High and COMPAT = High)

Table 7-10 provides the receiver, DDR timing specifications when TBIE is asserted high and COMPAT is asserted high.

Table 7-10. Receiver, DDR Timing Specification (TBIE = High and COMPAT = High)

Symbol	Characteristic [1]	Aligned Clock		Centered Clock		Unit	Note
		Min	Max	Min	Max		
T_1	Output valid time before rising edge of RECV_x_RCLK or RECV_x_RCLK_B	–0.500	0.500	1.440	—	ns	2
		–1.000	1.000	3.440	—	ns	3
T_2	Output valid time after rising edge of RECV_x_RCLK or RECV_x_RCLK_B	3.000	—	1.420	—	ns	2
		7.000	—	3.420	—	ns	3
T_3	RECV_x_RCLK or RECV_x_RCLK_B cycle time	15.800	16.200	15.800	—	ns	2
		31.800	32.200	31.800	—	ns	3
T_4	Rising edge of RECV_x_RCLK to rising edge of RECV_x_RCLK_B	7.800	8.200	7.800	8.200	ns	2
		15.800	16.200	15.800	16.200	ns	3
T_5	Falling edge of either clock to rising edge of other clock	–0.200	0.200	–0.200	0.200	ns	2
		–0.200	0.200	–0.200	0.200	ns	3

1 10 pF output load.

2 Full-speed, HSE = low.

3 Half-speed, HSE = high.

7.3.3 Reference Clock Timing

The following section provides the reference clock timing for the MC92603. Figure 7-7 provides the reference clock timing diagram.

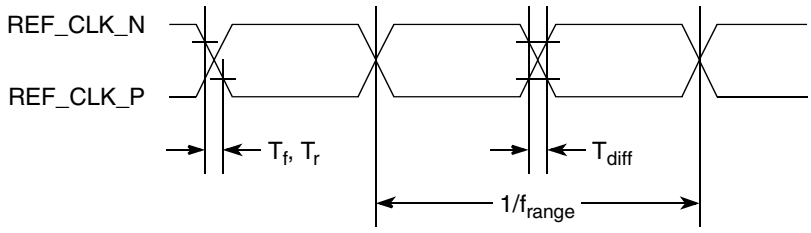


Figure 7-7. Reference Clock Timing Diagram

Table 7-11 provides the reference clock specifications.

Table 7-11. Reference Clock Specifications

Symbol	Characteristic	Min	Max	Unit
T_r	REF_CLK_P/N rise time [1]	—	2.0	ns
T_f	REF_CLK_P/N fall time [1]	—	2.0	ns
f_{range}	REF_CLK_P/N frequency range[2,3]	95	135	MHz
f_{range}	REF_CLK_P/N frequency range [2,4]	47.5	67.5	MHz
T_D	REF_CLK_P/N duty cycle	45	55	%
T_{diff}	REF_CLK_P to REF_CLK_N differential skew	—	1.0	ns
f_{tol}	REF_CLK_P/N frequency tolerance	–200	200	ppm
T_j	REF_CLK_P/N input jitter [5]	—	80	ps
T_{lock}	PLL lock time[6]	—	20,480 + 25 µs	bit-times

1 Measured between 10–90 percent points.
2 Measured between 50–50 percent points.
3 Full-speed operation (HSE = low).
4 Half-speed operation (HSE = high).
5 Total peak-to-peak jitter.
6 Lock time after compliant REF_CLK_P/N signal applied.

7.3.4 Serial Data Link Timing

The following section provides the serial data link timing for the MC92603. Figure 7-8 provides the link differential output timing diagram.

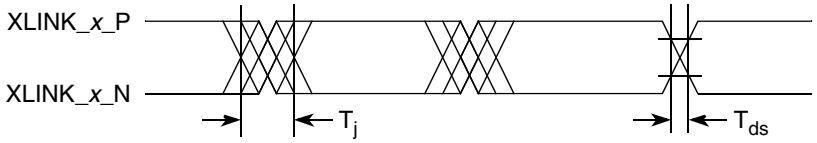


Figure 7-8. Link Differential Output Timing Diagram

Table 7-12 provides the link differential output timing specifications.

Table 7-12. Link Differential Output Specifications

Symbol	Characteristic	Min	Max	Unit
T_j	Total jitter [1]	—	0.24	UI
T_{dj}	Deterministic jitter [1]	—	0.12	UI
T_{ds}	Differential skew [1]	—	25	ps
X_{la}	Transmit latency [2]	—	57	bit-times

1 Measured between 50–50 percent points.

2 Rising edge XMIT_x_CLK to bit 0 transmit.

Figure 7-9 provides the link differential input timing diagram.

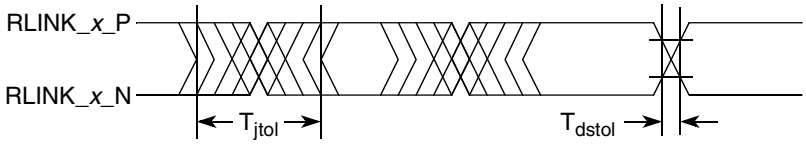


Figure 7-9. Link Differential Input Timing Diagram

Table 7-13 provides the link differential input timing specifications.

Table 7-13. Link Differential Input Timing Specifications

Symbol	Characteristic	Min	Max	Unit
T_r	Link input rise time[1]	300	—	ps
T_f	Link input fall time [1]	300	—	ps
T_{jtol}	Total jitter tolerance [2,3]	0.71	—	UI
T_{djtol}	Deterministic jitter tolerance [2, 3]	0.45	—	UI
T_{dstol}	Differential skew tolerance [2, 3]	175	—	ps
R_{lat}	Receive latency[4]	—	127	bit-times
T_{acq}	Receiver phase acquisition time	—	TBD [5]	bit-times

1 Measured between 10–90 percent points.

2 Measured between 50–50 percent points, 125 MHz REF_CLK, 1.25 Gbaud.

3 Per IEEE Std 802.3 specification [4].

4 Bit 0 at receiver input to parallel data out (RCCE = high, WSYNC1 and WSYNC0 = low).

5 Measured with worst-case eye opening, Idle pattern, and reference PLL locked.

7.3.5 MDIO Interface Timing

The following section provides the MDIO interface timing for the MC92603. Figure 7-10 provides the MDIO interface timing diagram.

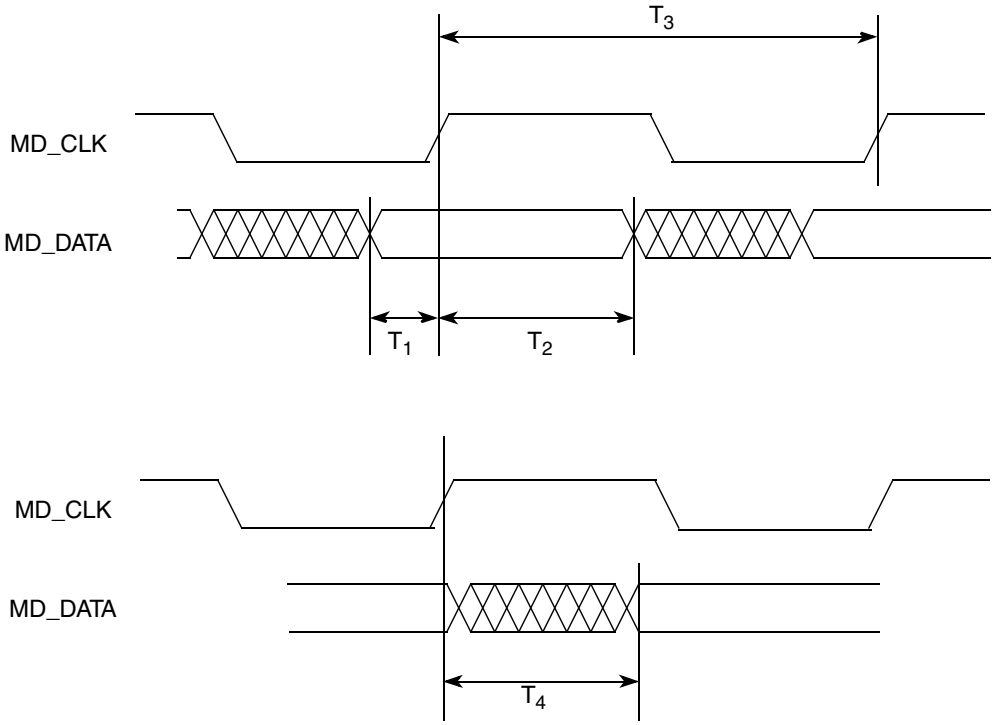


Figure 7-10. MDIO Interface Timing Diagram

Table 7-14 provides the MDIO interface timing specifications.

Table 7-14. MDIO Interface Timing Specifications

Symbol	Characteristic	Min	Max	Unit
T_1	Setup time prior to rising edge of MD_CLK	10	—	ns
T_2	Hold time after rising edge of MD_CLK	10	—	ns
T_3	MD_CLK period	100	—	ns
T_4	Turnaround delay time (MD_DATA sourced by PHY)[1]		25	ns

[1] Load = 470 pF.

7.3.6 JTAG Test Port Timing

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MC92604. Figure 7-11 provides the JTAG I/O Timing Diagram.

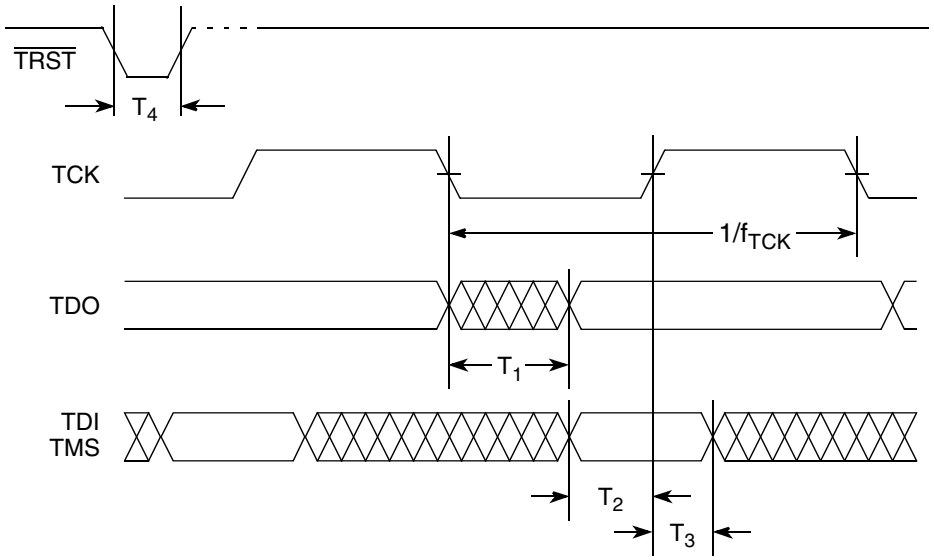


Figure 7-11. JTAG I/O Timing Diagram

Table 7-15 provides the JTAG I/O timing specifications.

Table 7-15. JTAG I/O Timing Specifications

Symbol	Characteristic	Min	Max	Unit
T_1	Output propagation time after falling edge of TCK[1]	1.0	8.0	ns
T_2	Setup time to rising edge of TCK	1.0	—	ns
T_3	Hold time to rising edge of TCK	0.5	—	ns
f_{TCK}	TCK frequency	—	20	MHz
T_D	TCK duty cycle	35	65	%
t_r, t_f	TCK input rise/fall time	—	2	ns
T_4	$\overline{TRST}$ assert pulse width	25	—	ns

1 10 pF output load

Chapter 8
Package Description

This chapter consists of the following sections:

The following section provides the package parameters and mechanical dimensions of the MC92603device. The MC92603 is offered in a 256 MAPBGA package. The 256 MAPBGA utilizes an aggressive 1 mm ball pitch and 17 mm body size for applications where board space is limited.

8.1 256 MAPBGA Package Parameter Summary

- Package Type—Fine pitch ball grid array
- Package Outline—17 mm x 17 mm
- Package Height—1.60 mm maximum
- Number of Balls—256
- Ball Pitch—1 mm
- Ball Diameter—0.40–0.60 mm

8.2 Nomenclature and Dimensions of the 256 MAPBGA Package

Figure 8-1 provides the bottom surface nomenclature and package outline drawing of the 256 MAPBGA package. Figure 8-2 provides the package dimensions. Figure 8-3 provides a graphic of the package pin signal mappings.

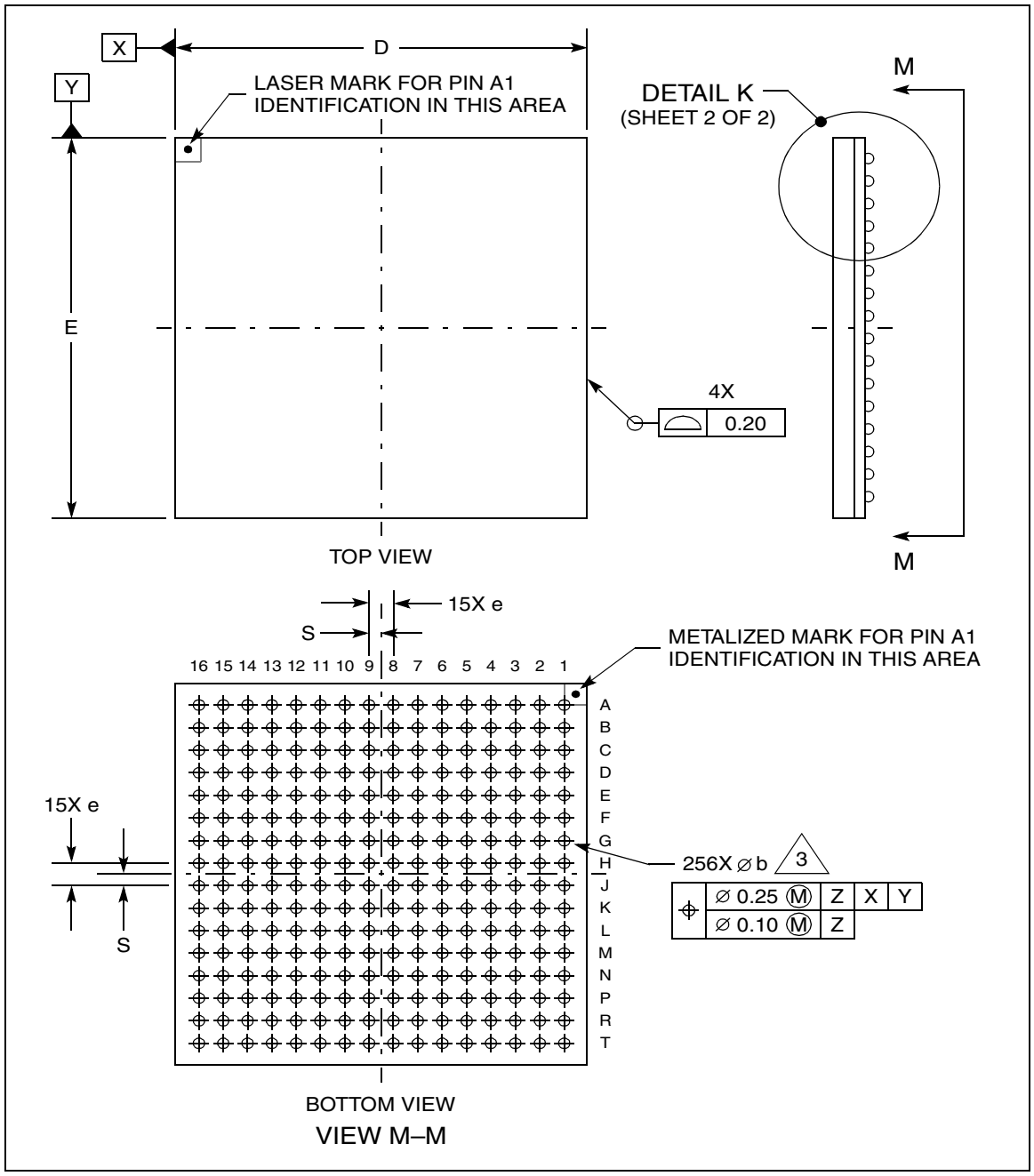
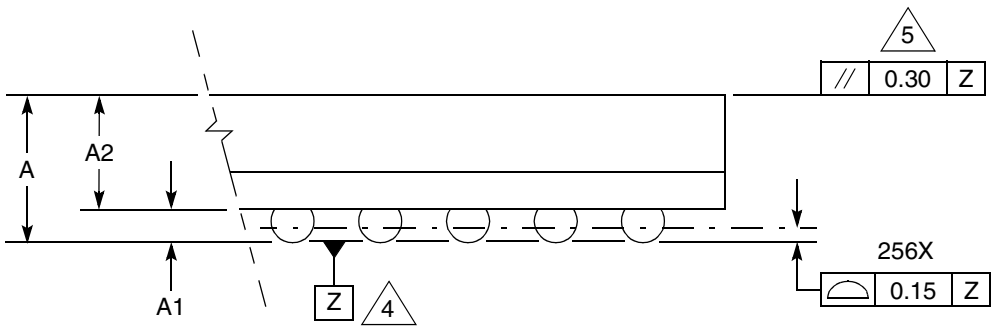


Figure 8-1. 256 MAPBGA Nomenclature



DETAIL K

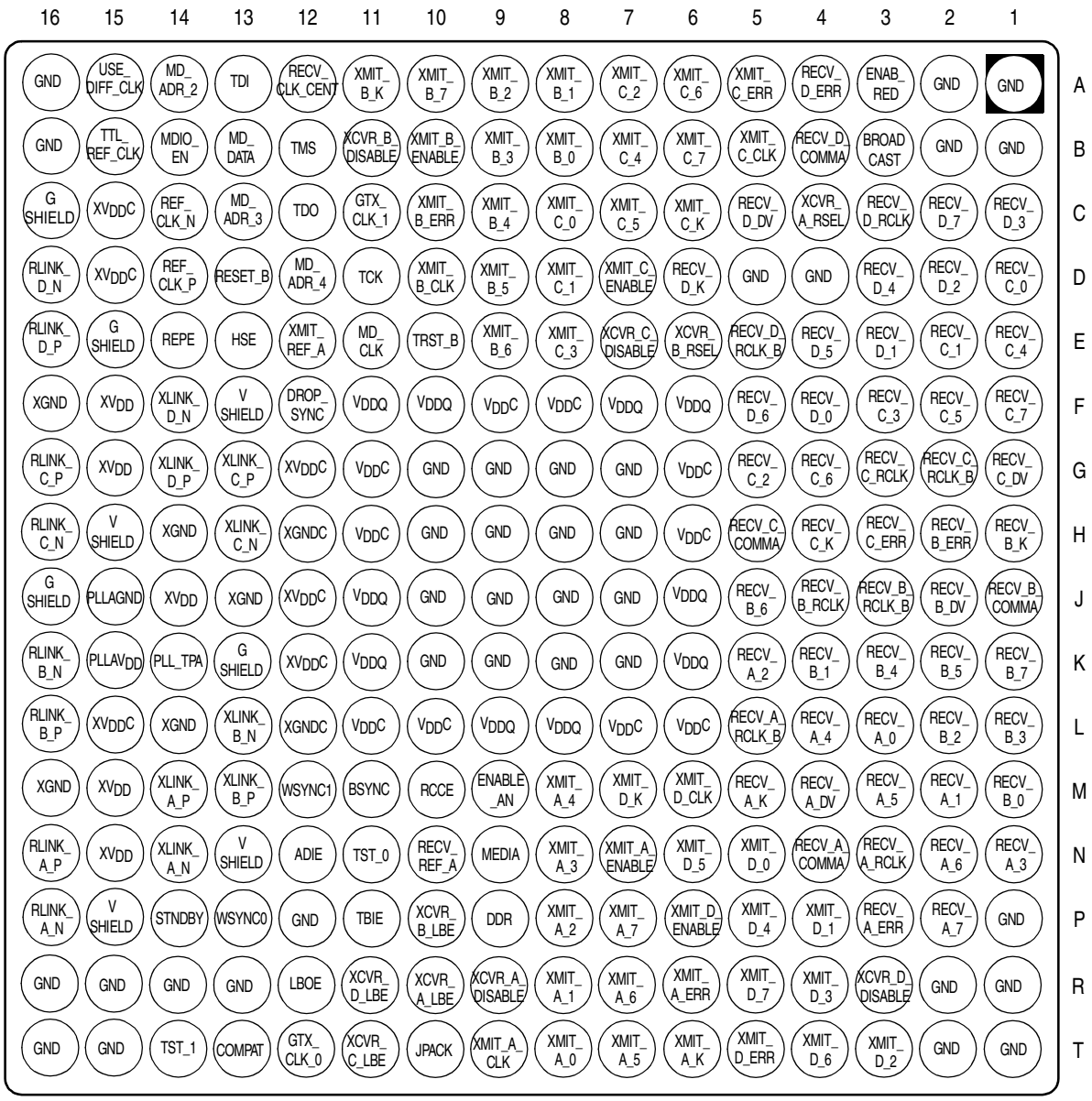
VIEW ROTATED 90° CLOCKWISE

DIM	MIN	MAX
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.40	0.60
D	17.00 BSC	
E	17.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

NOTES

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 8-2. 256 MAPBGA Dimensions



View M-M (Bottom View)

Figure 8-3. MC92603 Package Ball Mapping

8.3 Package Thermal Characteristics

Thermal values for the 256 pin MAPBGA are listed below in Table 8-1. The values listed below assume the customer will be mounting the packages on a thermally enhanced mother board. This is defined as a minimum 4-layer board with one ground plane. The values listed below were measured in accordance with established JEDEC (Joint Electron Device Engineering Council) standards.

Table 8-1. MC92603 Package Thermal Resistance Values

Symbol	Description	256 MAPBGA	Units
θ_{ja-0}	Thermal resistance from junction to ambient, still air	27	°C/W
θ_{ja-2}	Thermal resistance from junction to ambient, 200 LFM[1]	23	°C/W
θ_{ja-4}	Thermal resistance from junction to ambient, 400 LFM[1]	22	°C/W

[1] Airflow in linear feet per minute

8.4 MC92603Chip Pinout Listing

Table 8-2 list the MC92603signal to ball location mapping for the package. Also shown are signaling direction (input or output), and the type of logic interface.

Table 8-2. MC92603 Signal to Ball Mapping (Sheet 1 of 7)

Signal Name	Description	Ball Number (256 MAPBGA)	Direction	I/O Type
XMIT_A_CLK	Transmitter A, Interface Clock	T9	Input	LVTTL
XMIT_A_0	Transmitter A, Data bit 0	T8	Input	LVTTL
XMIT_A_1	Transmitter A, Data bit 1	R8	Input	LVTTL
XMIT_A_2	Transmitter A, Data bit 2	P8	Input	LVTTL
XMIT_A_3	Transmitter A, Data bit 3	N8	Input	LVTTL
XMIT_A_4	Transmitter A, Data bit 4	M8	Input	LVTTL
XMIT_A_5	Transmitter A, Data bit 5	T7	Input	LVTTL
XMIT_A_6	Transmitter A, Data bit 6	R7	Input	LVTTL
XMIT_A_7	Transmitter A, Data bit 7	P7	Input	LVTTL
XMIT_A_K	Transmitter A, K	T6	Input	LVTTL
XMIT_A_ERR	Transmitter A, Force Code Error	R6	Input	LVTTL
XMIT_A_ENABLE	Transmitter A, Enable Data In	N7	Input	LVTTL
XCVR_A_DISABLE	Transceiver A, Disable	R9	Input	LVTTL
RECV_A_0	Receiver A, Data bit 0	L3	Output	LVTTL
RECV_A_1	Receiver A, Data bit 1	M2	Output	LVTTL
RECV_A_2	Receiver A, Data bit 2	K5	Output	LVTTL
RECV_A_3	Receiver A, Data bit 3	N1	Output	LVTTL

Table 8-2. MC92603 Signal to Ball Mapping (Sheet 2 of 7)

Signal Name	Description	Ball Number (256 MAPBGA)	Direction	I/O Type
RECV_A_4	Receiver A, Data bit 4	L4	Output	LVTTL
RECV_A_5	Receiver A, Data bit 5	M3	Output	LVTTL
RECV_A_6	Receiver A, Data bit 6	N2	Output	LVTTL
RECV_A_7	Receiver A, Data bit 7	P2	Output	LVTTL
RECV_A_COMMA	Receiver A, COMMA Detect (status)	N4	Output	LVTTL
RECV_A_K	Receiver A, K (status)	M5	Output	LVTTL
RECV_A_DV	Receiver A, Data Valid (status)	M4	Output	LVTTL
RECV_A_ERR	Receiver A, Error Detect	P3	Output	LVTTL
RECV_A_RCLK	Receiver A, Receive Data Clock	N3	Output	LVTTL
RECV_A_RCLK_B	Receiver A, Data Clock Complement	L5	Output	LVTTL
RLINK_A_P	Receiver A, Positive Link Input	N16	Input	Link
RLINK_A_N	Receiver A, Negative Link Input	P16	Input	Link
XLINK_A_P	Transmitter A, Positive Link Out	M14	Output	Link
XLINK_A_N	Transmitter A, Negative Link Out	N14	Output	Link
XMIT_B_CLK	Transmitter B, Interface Clock	D10	Input	LVTTL
XMIT_B_0	Transmitter B, Data bit 0	B8	Input	LVTTL
XMIT_B_1	Transmitter B, Data bit 1	A8	Input	LVTTL
XMIT_B_2	Transmitter B, Data bit 2	A9	Input	LVTTL
XMIT_B_3	Transmitter B, Data bit 3	B9	Input	LVTTL
XMIT_B_4	Transmitter B, Data bit 4	C9	Input	LVTTL
XMIT_B_5	Transmitter B, Data bit 5	D9	Input	LVTTL
XMIT_B_6	Transmitter B, Data bit 6	E9	Input	LVTTL
XMIT_B_7	Transmitter B, Data bit 7	A10	Input	LVTTL
XMIT_B_K	Transmitter B, K	A11	Input	LVTTL
XMIT_B_ERR	Transmitter B, Force Code Error	C10	Input	LVTTL
XMIT_B_ENABLE	Transmitter B, Enable Data In	B10	Input	LVTTL
XCVR_B_DISABLE	Transceiver B, Disable	B11	Input	LVTTL
RECV_B_0	Receiver B, Data bit 0	M1	Output	LVTTL
RECV_B_1	Receiver B, Data bit 1	K4	Output	LVTTL
RECV_B_2	Receiver B, Data bit 2	L2	Output	LVTTL
RECV_B_3	Receiver B, Data bit 3	L1	Output	LVTTL
RECV_B_4	Receiver B, Data bit 4	K3	Output	LVTTL

Table 8-2. MC92603 Signal to Ball Mapping (Sheet 3 of 7)

Signal Name	Description	Ball Number (256 MAPBGA)	Direction	I/O Type
RECV_B_5	Receiver B, Data bit 5	K2	Output	LVTTL
RECV_B_6	Receiver B, Data bit 6	J5	Output	LVTTL
RECV_B_7	Receiver B, Data bit 7	K1	Output	LVTTL
RECV_B_COMMA	Receiver B, COMMA Detect (status)	J1	Output	LVTTL
RECV_B_K	Receiver B, K (status)	H1	Output	LVTTL
RECV_B_DV	Receiver B, Data Valid (status)	J2	Output	LVTTL
RECV_B_ERR	Receiver B, Error Detect	H2	Output	LVTTL
RECV_B_RCLK	Receiver B, Receive Data Clock	J4	Output	LVTTL
RECV_B_RCLK_B	Receiver B, Data Clock Complement	J3	Output	LVTTL
RLINK_B_P	Receiver B, Positive Link Input	L16	Input	Link
RLINK_B_N	Receiver B, Negative Link Input	K16	Input	Link
XLINK_B_P	Transmitter B, Positive Link Out	M13	Output	Link
XLINK_B_N	Transmitter B, Negative Link Out	L13	Output	Link
XMIT_C_CLK	Transmitter C, Interface Clock	B5	Input	LVTTL
XMIT_C_0	Transmitter C, Data bit 0	C8	Input	LVTTL
XMIT_C_1	Transmitter C, Data bit 1	D8	Input	LVTTL
XMIT_C_2	Transmitter C, Data bit 2	A7	Input	LVTTL
XMIT_C_3	Transmitter C, Data bit 3	E8	Input	LVTTL
XMIT_C_4	Transmitter C, Data bit 4	B7	Input	LVTTL
XMIT_C_5	Transmitter C, Data bit 5	C7	Input	LVTTL
XMIT_C_6	Transmitter C, Data bit 6	A6	Input	LVTTL
XMIT_C_7	Transmitter C, Data bit 7	B6	Input	LVTTL
XMIT_C_K	Transmitter C, K	C6	Input	LVTTL
XMIT_C_ERR	Transmitter C, Force Code Error	A5	Input	LVTTL
XMIT_C_ENABLE	Transmitter C, Enable Data In	D7	Input	LVTTL
XCVR_C_DISABLE	Transceiver C, Disable	E7	Input	LVTTL
RECV_C_0	Receiver C, Data bit 0	D1	Output	LVTTL
RECV_C_1	Receiver C, Data bit 1	E2	Output	LVTTL
RECV_C_2	Receiver C, Data bit 2	G5	Output	LVTTL
RECV_C_3	Receiver C, Data bit 3	F3	Output	LVTTL
RECV_C_4	Receiver C, Data bit 4	E1	Output	LVTTL
RECV_C_5	Receiver C, Data bit 5	F2	Output	LVTTL

Table 8-2. MC92603 Signal to Ball Mapping (Sheet 4 of 7)

Signal Name	Description	Ball Number (256 MAPBGA)	Direction	I/O Type
RECV_C_6	Receiver C, Data bit 6	G4	Output	LVTTL
RECV_C_7	Receiver C, Data bit 7	F1	Output	LVTTL
RECV_C_COMMA	Receiver C, COMMA Detect (status)	H5	Output	LVTTL
RECV_C_K	Receiver C, K (status)	H4	Output	LVTTL
RECV_C_DV	Receiver C Data Valid (status)	G1	Output	LVTTL
RECV_C_ERR	Receiver C, Error Detect	H3	Output	LVTTL
RECV_C_RCLK	Receiver C, Receive Data Clock	G3	Output	LVTTL
RECV_C_RCLK_B	Receiver C, Data Clock Complement	G2	Output	LVTTL
RLINK_C_P	Receiver C, Positive Link Input	G16	Input	Link
RLINK_C_N	Receiver C, Negative Link Input	H16	Input	Link
XLINK_C_P	Transmitter C, Positive Link Out	G13	Output	Link
XLINK_C_N	Transmitter C, Negative Link Out	H13	Output	Link
XMIT_D_CLK	Transmitter D, Interface Clock	M6	Input	LVTTL
XMIT_D_0	Transmitter D, Data bit 0	N5	Input	LVTTL
XMIT_D_1	Transmitter D, Data bit 1	P4	Input	LVTTL
XMIT_D_2	Transmitter D, Data bit 2	T3	Input	LVTTL
XMIT_D_3	Transmitter D, Data bit 3	R4	Input	LVTTL
XMIT_D_4	Transmitter D, Data bit 4	P5	Input	LVTTL
XMIT_D_5	Transmitter D, Data bit 5	N6	Input	LVTTL
XMIT_D_6	Transmitter D, Data bit 6	T4	Input	LVTTL
XMIT_D_7	Transmitter D, Data bit 7	R5	Input	LVTTL
XMIT_D_K	Transmitter D, K	M7	Input	LVTTL
XMIT_D_ERR	Transmitter D, Force Code Error	T5	Input	LVTTL
XMIT_D_ENABLE	Transmitter D, Enable Data In	P6	Input	LVTTL
XCVR_D_DISABLE	Transceiver D, Disable	R3	Input	LVTTL
RECV_D_0	Receiver D, Data bit 0	F4	Output	LVTTL
RECV_D_1	Receiver D, Data bit 1	E3	Output	LVTTL
RECV_D_2	Receiver D, Data bit 2	D2	Output	LVTTL
RECV_D_3	Receiver D, Data bit 3	C1	Output	LVTTL
RECV_D_4	Receiver D, Data bit 4	D3	Output	LVTTL
RECV_D_5	Receiver D, Data bit 5	E4	Output	LVTTL
RECV_D_6	Receiver D, Data bit 6	F5	Output	LVTTL

Table 8-2. MC92603 Signal to Ball Mapping (Sheet 5 of 7)

Signal Name	Description	Ball Number (256 MAPBGA)	Direction	I/O Type
RECV_D_7	Receiver D, Data bit 7	C2	Output	LVTTL
RECV_D_COMMA	Receiver D, COMMA Detect (status)	B4	Output	LVTTL
RECV_D_K	Receiver D, K (status)	D6	Output	LVTTL
RECV_D_DV	Receiver D, Data Valid (status)	C5	Output	LVTTL
RECV_D_ERR	Receiver D, Error Detect	A4	Output	LVTTL
RECV_D_RCLK	Receiver D, Receive Data Clock	C3	Output	LVTTL
RECV_D_RCLK_B	Receiver D, Data Clock Complement	E5	Output	LVTTL
RLINK_D_P	Receiver D, Positive Link Input	E16	Input	Link
RLINK_D_N	Receiver D, Negative Link Input	D16	Input	Link
XLINK_D_P	Transmitter D, Positive Link Out	G14	Output	Link
XLINK_D_N	Transmitter D, Negative Link Out	F14	Output	Link
DROP_SYNC	Drop Synchronization	F12	Input	LVTTL
TBIE	Ten-Bit Interface Enable	P11	Input	LVTTL
HSE	Half Speed Enable	E13	Input	LVTTL
BSYNC	Byte Synchronization Mode	M11	Input	LVTTL
ADIE	Add/Drop *IDLE* Enable	N12	Input	LVTTL
COMPAT	IEEE 802.3 Compatibility Mode	T13	Input	LVTTL
DDR	Enable Double Data Rate	P9	Input	LVTTL
ENABLE_AN	Enable Auto-Negotiate if in GMII Mode	M9	Input	LVTTL
REPE	Repeater Mode Enable	E14	Input	LVTTL
REF_CLK_P	PECL Reference Clock Positive Input	D14	Input	LVPECL
REF_CLK_N	PECL Reference Clock Negative Input	C14	Input	LVPECL
TTL_REF_CLK	TTL Reference Clock Input	B15	Input	LVTTL
USE_DIFF_CLK	Select reference Clock Input	A15	Input	LVTTL
RCCE	Recovered Clock Enable	M10	Input	LVTTL
GTX_CLK0	Buffered Reference Clock Output	T12	Output	LVTTL
GTX_CLK1	Buffered Reference Clock Output	C11	Output	LVTTL
RECV_REF_A	Use Receiver A as Primary Clock	N10	Input	LVTTL
XMIT_REF_A	Use Transmitter A as Primary Clock	E12	Input	LVTTL
PLL_TPA[1]	PLL Analog Test Point	K14	Output	Analog
TST_0	Test Mode Select 0	N11	Input	LVTTL
TST_1	Test Mode Select 1	T14	Input	LVTTL

Table 8-2. MC92603 Signal to Ball Mapping (Sheet 6 of 7)

Signal Name	Description	Ball Number (256 MAPBGA)	Direction	I/O Type
XCVR_A_LBE	Loopback Enable Channel A	R10	Input	LVTTL
XCVR_B_LBE	Loopback Enable Channel B	P10	Input	LVTTL
XCVR_C_LBE	Loopback Enable Channel C	T11	Input	LVTTL
XCVR_D_LBE	Loopback Enable Channel D	R11	Input	LVTTL
LBOE	Loopback Output Enable	R12	Input	LVTTL
STNDBY	Standby Mode Enable	P14	Input	LVTTL
MEDIA	Media Impedance Select	N9	Input	LVTTL
RECV_CLK_CENT	Center Recov. Clock Relative to Data	A12	Input	LVTTL
JPACK	Enable Jumbo Packets	T10	Input	LVTTL
WSYNC1	Word Sync Definer	M12	Input	LVTTL
WSYNC0	Word Sync Definer	P13	Input	LVTTL
TMS	JTAG Test Mode Select	B12	Input	LVTTL
TDI	JTAG Test Data In	A13	Input	LVTTL
TRST_B	JTAG Test Reset Bar	E10	Input	LVTTL
TCK	JTAG Test Clock	D11	Input	LVTTL
TDO	JTAG Test Data Out	C12	Output	LVTTL
MDIO_EN	MDIO Enable	B14	Input	LVTTL
MD_CLK	MDIO Clock	E11	Input	LVTTL
MD_DATA	MDIO Data	B13	Bidirectional	LVTTL
MD_ADR4	MDIO Phy Address Bit 4	D12	Input	LVTTL
MD_ADR3	MDIO Phy Address Bit 3	C13	Input	LVTTL
MD_ADR2	MDIO Phy Address Bit 2	A14	Input	LVTTL
RESET_B	System Reset Bar	D13	Input	LVTTL
ENAB_RED	Enable Redundant Links	A3	Input	LVTTL
BROADCAST	Transmit over both links	B3	Input	LVTTL
XCVR_A_RSEL	Use XLINK_C and RLINK_C	C4	Input	LVTTL
XCVR_B_RSEL	Use XLINK_D and RLINK_D	E6	Input	LVTTL

Table 8-2. MC92603 Signal to Ball Mapping (Sheet 7 of 7)

Signal Name	Description	Ball Number (256 MAPBGA)	Direction	I/O Type
$V_{DD}C$	Core Logic Supply (10)	F8-9, G6, G11, H6, H11, L6-7,L10-11	V_{DD}	Supply
GND	Core Logic Ground/ (36) LVTTL/CMOS I/O Ground	A1-2, A16, B1-2, B16, D4-5, G7-10, H7-10, J7-10, K7-10, P1, P12, R1-2, R13-16, T1-2, T15-16	GND	Ground
$PLLAV_{DD}$	PLL Analog Supply (1)	K15	AV_{DD}	Supply
PLLAGND	PLL Analog Ground (1)	J15	GND	Ground
V_{DDQ}	LVTTL/CMOS I/O Supply (10)	F6-7, F10-11, J6, J11, K6, K11, L8-9	V_{DDQ}	Supply
XV_{DD}	Link I/O Supply (5)	F15, G15, J14, M15, N15	XV_{DD}	Supply
XGND	Link I/O Ground (5)	F16, H14, J13, L14, M16	GND	Ground
$XV_{DD}C$	Core Analog Logic Supply (6)	C15, D15, G12, J12, K12, L15	XV_{DD}	Supply
XGNDC	Core Analog Ground (2)	H12, L12	GND	Ground
V SHIELD	Link V_{DD} Shield (4)	F13, H15, N13, P15	XV_{DD}	Supply
G SHIELD	Link Ground Shield (4)	C16, E15, J16, K13	GND	Ground

[1] Ball K14 (PLL_TPA) should be left unterminated. It is used for manufacturing test only.

Appendix A
Ordering Information

Figure A-1 provides the Freescale part numbering nomenclature for the MC92603 Quad Gigabit Ethernet transceiver. For product availability, contact your local Freescale Semiconductor sales representative.

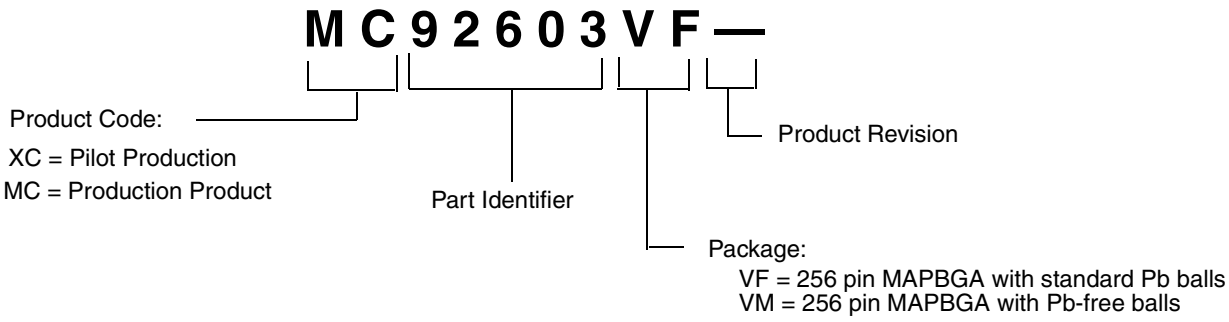


Figure A-1. Freescale Part Number Key

Appendix B
8B/10B Coding Scheme

The MC92603 provides fibre channel-specific 8B/10B encoding and decoding based on the FC-1 fibre channel standard. Given 8 bits entering a channel, the 8B/10B encoding converts them to 10 bits thereby increasing the transition density of the serially transmitted signal.

B.1 Overview

The FC-1 standard applies an algorithm that ensures that no more than five 1s or 0s are transmitted consecutively, giving a transition density equal to 2.5 for each 10-bit data block. Such a density ensures proper DC balance across the link and is sufficient for good clock recovery.

In the 8B/10B notation scheme, bytes are referred to as transmission characters, and each bit is represented by letters. Unencoded bits, the 8 bits that have not passed through a 8B/10B encoder, are represented by letters ‘A’ through ‘H,’ which are bits 0 through 7.

One unencoded transmission character (Byte)							
H	G	F	E	D	C	B	A
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
							¦ lsb

Figure B-1. Unencoded Transmission Character Bit Ordering

Encoded bits, those that have passed through an encoder, are represented with the letters ‘a’ through ‘j,’ representing bits 0–9, respectively. Character (bit) ordering in the fibre channel nomenclature is little-endian, with ‘a’ being the least significant bit in a byte.

One coded transmission character (Byte)									
j	h	g	f	i	e	d	c	b	a
Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
									¦ lsb

Figure B-2. Encoded Transmission Character Bit Ordering

B.1.1 Naming Transmission Characters

Transmission characters are given names based on the type of data in the byte and the bit values of the character. Two types of transmission characters are specified: data and special. Data characters are labeled ‘D’ characters and special characters are labeled ‘K’ characters. Each transmission character has a bit value and a corresponding decimal value. These elements are combined to provide each character with a name, see Table B-1.

Table B-1. Components of a Character Name

H G F	E D C B A	8B/10B notation
0 0 1	1 1 1 0 0	Data bit value
1	28	Decimal value of the bit value
D or K		Kind of transmission character
D28.1 = Data name assigned to this data byte if it is a data character. K28.1 = Data name assigned to this data byte if it is a special character.		

B.1.2 Encoding

Following is a simplified sequence of steps in 8B/10B coding:

1. An 8-bit block of unencoded data (a transmission character) is picked up by a transmitter.
2. The transmission character is broken into sub-blocks of 3 bits and 5 bits. The letters H, G, and F comprise the 3-bit block, and the letters E, D, C, B, and A comprise the 5-bit block.
3. The 3- and 5-bit sub-blocks pass through a 3B/4B encoder and a 5B/6B encoder, respectively. A bit is added to each sub-block, such that the transmission character is encoded and expanded to a total of 10 bits.
4. At the time the character is expanded into 10 bits, it is also encoded into the proper running disparity, either positive (RD+) or negative (RD-) depending on certain calculations (see Section B.1.3, “Calculating Running Disparity”). At startup, the transmitter assumes negative running disparity.
5. The positive or negative disparity transmission character (see Figure B-3) is passed to the transmit driver, available for differentialization (see Section 2.3.1, “Transmit Driver Operation”).

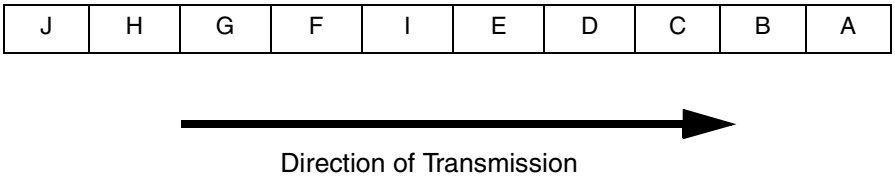


Figure B-3. Character Transmission

B.1.3 Calculating Running Disparity

Running disparity improves error detection and recovery. The rules for calculating the running disparity for sub-blocks are as follows (reference *Fibre Channel, Gigabit Communications and I/O for Computer Networks*):

- Running disparity at the end of any sub-block is positive if (1) the encoded sub-block contains more 1s than 0s, (2) if the 6-bit sub-block is 6'b00 0111, or (3) if the 4-bit sub-block is 4'b0011.
- Running disparity at the end of any sub-block is negative if (1) the encoded sub-block contains more 0 than 1 bits, (2) if the 6-bit sub-block is 6'b11 1000, or (3) if the 4-bit sub-block is 4'b1100.
- Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

B.2 Data Tables

Table B-2 displays the full valid data character 8B/10B codes. The values in the 'Data Value HGFEDCBA' column are the possible bit values of the unencoded transmission characters. The current RD values are the possible positive and negative running disparity values.

Table B-2. Valid Data Characters (Sheet 1 of 4)

Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D0.0	000 00000	100111 0100	011000 1011	D0.1	001 00000	100111 1001	011000 1001
D1.0	000 00001	011101 0100	100010 1011	D1.1	001 00001	011101 1001	100010 1001
D2.0	000 00010	101101 0100	010010 1011	D2.1	001 00010	101101 1001	010010 1001
D3.0	000 00011	110001 1011	110001 0100	D3.1	001 00011	110001 1001	110001 1001
D4.0	000 00100	110101 0100	001010 1011	D4.1	001 00100	110101 1001	001010 1001
D5.0	000 00101	101001 1011	101001 0100	D5.1	001 00101	101001 1001	101001 1001
D6.0	000 00110	011001 1011	011001 0100	D6.1	001 00110	011001 1001	011001 1001
D7.0	000 00111	111000 1011	000111 0100	D7.1	001 00111	111000 1001	000111 1001
D8.0	000 01000	111001 0100	000110 1011	D8.1	001 01000	111001 1001	000110 1001
D9.0	000 01001	100101 1011	100101 0100	D9.1	001 01001	100101 1001	100101 1001
D10.0	000 01010	010101 1011	010101 0100	D10.1	001 01010	010101 1001	010101 1001
D11.0	000 01011	110100 1011	110100 0100	D11.1	001 01011	110100 1001	110100 1001
D12.0	000 01100	001101 1011	001101 0100	D12.1	001 01100	001101 1001	001101 1001
D13.0	000 01101	101100 1011	101100 0100	D13.1	001 01101	101100 1001	101100 1001
D14.0	000 01110	011100 1011	011100 0100	D14.1	001 01110	011100 1001	011100 1001
D15.0	000 01111	010111 0100	101000 1011	D15.1	001 01111	010111 1001	101000 1001
D16.0	000 10000	011011 0100	100100 1011	D16.1	001 10000	011011 1001	100100 1001
D17.0	000 10001	100011 1011	100011 0100	D17.1	001 10001	100011 1001	100011 1001
D18.0	000 10010	010011 1011	010011 0100	D18.1	001 10010	010011 1001	010011 1001
D19.0	000 10011	110010 1011	110010 0100	D19.1	001 10011	110010 1001	110010 1001
D20.0	000 10100	001011 1011	001011 0100	D20.1	001 10100	001011 1001	001011 1001
D21.0	000 10101	101010 1011	101010 0100	D21.1	001 10101	101010 1001	101010 1001
D22.0	000 10110	011010 1011	011010 0100	D22.1	001 10110	011010 1001	011010 1001
D23.0	000 10111	111010 0100	000101 1011	D23.1	001 10111	111010 1001	000101 1001
D24.0	000 11000	110011 0100	001100 1011	D24.1	001 11000	110011 1001	001100 1001
D25.0	000 11001	100110 1011	100110 0100	D25.1	001 11001	100110 1001	100110 1001
D26.0	000 11010	010110 1011	010110 0100	D26.1	001 11010	010110 1001	010110 1001
D27.0	000 11011	110110 0100	001001 1011	D27.1	001 11011	110110 1001	001001 1001
D28.0	000 11100	001110 1011	001110 0100	D28.1	001 11100	001110 1001	001110 1001
D29.0	000 11101	101110 0100	010001 1011	D29.1	001 11101	101110 1001	010001 1001
D30.0	000 11110	011110 0100	100001 1011	D30.1	001 11110	011110 1001	100001 1001
D31.0	000 11111	101011 0100	010100 1011	D31.1	001 11111	101011 1001	010100 1001

Table B-2. Valid Data Characters (Sheet 2 of 4)

Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D0.2	010 00000	100111 0101	011000 0101	D0.3	011 00000	100111 0011	011000 1100
D1.2	010 00001	011101 0101	100010 0101	D1.3	011 00001	011101 0011	100010 1100
D2.2	010 00010	101101 0101	010010 0101	D2.3	011 00010	101101 0011	010010 1100
D3.2	010 00011	110001 0101	110001 0101	D3.3	011 00011	110001 1100	110001 0011
D4.2	010 00100	110101 0101	001010 0101	D4.3	011 00100	110101 0011	001010 1100
D5.2	010 00101	101001 0101	101001 0101	D5.3	011 00101	101001 1100	101001 0011
D6.2	010 00110	011001 0101	011001 0101	D6.3	011 00110	011001 1100	011001 0011
D7.2	010 00111	111000 0101	000111 0101	D7.3	011 00111	111000 1100	000111 0011
D8.2	010 01000	111001 0101	000110 0101	D8.3	011 01000	111001 0011	000110 1100
D9.2	010 01001	100101 0101	100101 0101	D9.3	011 01001	100101 1100	100101 0011
D10.2	010 01010	010101 0101	010101 0101	D10.3	011 01010	010101 1100	010101 0011
D11.2	010 01011	110100 0101	110100 0101	D11.3	011 01011	110100 1100	110100 0011
D12.2	010 01100	001101 0101	001101 0101	D12.3	011 01100	001101 1100	001101 0011
D13.2	010 01101	101100 0101	101100 0101	D13.3	011 01101	101100 1100	101100 0011
D14.2	010 01110	011100 0101	011100 0101	D14.3	011 01110	011100 1100	011100 0011
D15.2	010 01111	010111 0101	101000 0101	D15.3	011 01111	010111 0011	101000 1100
D16.2	010 10000	011011 0101	100100 0101	D16.3	011 10000	011011 0011	100100 1100
D17.2	010 10001	100011 0101	100011 0101	D17.3	011 10001	100011 1100	100011 0011
D18.2	010 10010	010011 0101	010011 0101	D18.3	011 10010	010011 1100	010011 0011
D19.2	010 10011	110010 0101	110010 0101	D19.3	011 10011	110010 1100	110010 0011
D20.2	010 10100	001011 0101	001011 0101	D20.3	011 10100	001011 1100	001011 0011
D21.2	010 10101	101010 0101	101010 0101	D21.3	011 10101	101010 1100	101010 0011
D22.2	010 10110	011010 0101	011010 0101	D22.3	011 10110	011010 1100	011010 0011
D23.2	010 10111	111010 0101	000101 0101	D23.3	011 10111	111010 0011	000101 1100
D24.2	010 11000	110011 0101	001100 0101	D24.3	011 11000	110011 0011	001100 1100
D25.2	010 11001	100110 0101	100110 0101	D25.3	011 11001	100110 1100	100110 0011
D26.2	010 11010	010110 0101	010110 0101	D26.3	011 11010	010110 1100	010110 0011
D27.2	010 11011	110110 0101	001001 0101	D27.3	011 11011	110110 0011	001001 1100
D28.2	010 11100	001110 0101	001110 0101	D28.3	011 11100	001110 1100	001110 0011
D29.2	010 11101	101110 0101	010001 0101	D29.3	011 11101	101110 0011	010001 1100
D30.2	010 11110	011110 0101	100001 0101	D30.3	011 11110	011110 0011	100001 1100
D31.2	010 11111	101011 0101	010100 0101	D31.3	011 11111	101011 0011	010100 1100

Table B-2. Valid Data Characters (Sheet 3 of 4)

Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D0.4	100 00000	100111 0010	011000 1101	D0.5	101 00000	100111 1010	011000 1010
D1.4	100 00001	011101 0010	100010 1101	D1.5	101 00001	011101 1010	100010 1010
D2.4	100 00010	101101 0010	010010 1101	D2.5	101 00010	101101 1010	010010 1010
D3.4	100 00011	110001 1101	110001 0010	D3.5	101 00011	110001 1010	110001 1010
D4.4	100 00100	110101 0010	001010 1101	D4.5	101 00100	110101 1010	001010 1010
D5.4	100 00101	101001 1101	101001 0010	D5.5	101 00101	101001 1010	101001 1010
D6.4	100 00110	011001 1101	011001 0010	D6.5	101 00110	011001 1010	011001 1010
D7.4	100 00111	111000 1101	000111 0010	D7.5	101 00111	111000 1010	000111 1010
D8.4	100 01000	111001 0010	000110 1101	D8.5	101 01000	111001 1010	000110 1010
D9.4	100 01001	100101 1101	100101 0010	D9.5	101 01001	100101 1010	100101 1010
D10.4	100 01010	010101 1101	010101 0010	D10.5	101 01010	010101 1010	010101 1010
D11.4	100 01011	110100 1101	110100 0010	D11.5	101 01011	110100 1010	110100 1010
D12.4	100 01100	001101 1101	001101 0010	D12.5	101 01100	001101 1010	001101 1010
D13.4	100 01101	101100 1101	101100 0010	D13.5	101 01101	101100 1010	101100 1010
D14.4	100 01110	011100 1101	011100 0010	D14.5	101 01110	011100 1010	011100 1010
D15.4	100 01111	010111 0010	101000 1101	D15.5	101 01111	010111 1010	101000 1010
D16.4	100 10000	011011 0010	100100 1101	D16.5	101 10000	011011 1010	100100 1010
D17.4	100 10001	100011 1101	100011 0010	D17.5	101 10001	100011 1010	100011 1010
D18.4	100 10010	010011 1101	010011 0010	D18.5	101 10010	010011 1010	010011 1010
D19.4	100 10011	110010 1101	110010 0010	D19.5	101 10011	110010 1010	110010 1010
D20.4	100 10100	001011 1101	001011 0010	D20.5	101 10100	001011 1010	001011 1010
D21.4	100 10101	101010 1101	101010 0010	D21.5	101 10101	101010 1010	101010 1010
D22.4	100 10110	011010 1101	011010 0010	D22.5	101 10110	011010 1010	011010 1010
D23.4	100 10111	111010 0010	000101 1101	D23.5	101 10111	111010 1010	000101 1010
D24.4	100 11000	110011 0010	001100 1101	D24.5	101 11000	110011 1010	001100 1010
D25.4	100 11001	100110 1101	100110 0010	D25.5	101 11001	100110 1010	100110 1010
D26.4	100 11010	010110 1101	010110 0010	D26.5	101 11010	010110 1010	010110 1010
D27.4	100 11011	110110 0010	001001 1101	D27.5	101 11011	110110 1010	001001 1010
D28.4	100 11100	001110 1101	001110 0010	D28.5	101 11100	001110 1010	001110 1010
D29.4	100 11101	101110 0010	010001 1101	D29.5	101 11101	101110 1010	010001 1010
D30.4	100 11110	011110 0010	100001 1101	D30.5	101 11110	011110 1010	100001 1010
D31.4	100 11111	101011 0010	010100 1101	D31.5	101 11111	101011 1010	010100 1010

Table B-2. Valid Data Characters (Sheet 4 of 4)

Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D0.6	110 00000	100111 0110	011000 0110	D0.7	111 00000	100111 0001	011000 1110
D1.6	110 00001	011101 0110	100010 0110	D1.7	111 00001	011101 0001	100010 1110
D2.6	110 00010	101101 0110	010010 0110	D2.7	111 00010	101101 0001	010010 1110
D3.6	110 00011	110001 0110	110001 0110	D3.7	111 00011	110001 1110	110001 0001
D4.6	110 00100	110101 0110	001010 0110	D4.7	111 00100	110101 0001	001010 1110
D5.6	110 00101	101001 0110	101001 0110	D5.7	111 00101	101001 1110	101001 0001
D6.6	110 00110	011001 0110	011001 0110	D6.7	111 00110	011001 1110	011001 0001
D7.6	110 00111	111000 0110	000111 0110	D7.7	111 00111	111000 1110	000111 0001
D8.6	110 01000	111001 0110	000110 0110	D8.7	111 01000	111001 0001	000110 1110
D9.6	110 01001	100101 0110	100101 0110	D9.7	111 01001	100101 1110	100101 0001
D10.6	110 01010	010101 0110	010101 0110	D10.7	111 01010	010101 1110	010101 0001
D11.6	110 01011	110100 0110	110100 0110	D11.7	111 01011	110100 1110	110100 1000
D12.6	110 01100	001101 0110	001101 0110	D12.7	111 01100	001101 1110	001101 0001
D13.6	110 01101	101100 0110	101100 0110	D13.7	111 01101	101100 1110	101100 1000
D14.6	110 01110	011100 0110	011100 0110	D14.7	111 01110	011100 1110	011100 1000
D15.6	110 01111	010111 0110	101000 0110	D15.7	111 01111	010111 0001	101000 1110
D16.6	110 10000	011011 0110	100100 0110	D16.7	111 10000	011011 0001	100100 1110
D17.6	110 10001	100011 0110	100011 0110	D17.7	111 10001	100011 0111	100011 0001
D18.6	110 10010	010011 0110	010011 0110	D18.7	111 10010	010011 0111	010011 0001
D19.6	110 10011	110010 0110	110010 0110	D19.7	111 10011	110010 1110	110010 0001
D20.6	110 10100	001011 0110	001011 0110	D20.7	111 10100	001011 0111	001011 0001
D21.6	110 10101	101010 0110	101010 0110	D21.7	111 10101	101010 1110	101010 0001
D22.6	110 10110	011010 0110	011010 0110	D22.7	111 10110	011010 1110	011010 0001
D23.6	110 10111	111010 0110	000101 0110	D23.7	111 10111	111010 0001	000101 1110
D24.6	110 11000	110011 0110	001100 0110	D24.7	111 11000	110011 0001	001100 1110
D25.6	110 11001	100110 0110	100110 0110	D25.7	111 11001	100110 1110	100110 0001
D26.6	110 11010	010110 0110	010110 0110	D26.7	111 11010	010110 1110	010110 0001
D27.6	110 11011	110110 0110	001001 0110	D27.7	111 11011	110110 0001	001001 1110
D28.6	110 11100	001110 0110	001110 0110	D28.7	111 11100	001110 1110	001110 0001
D29.6	110 11101	101110 0110	010001 0110	D29.7	111 11101	101110 0001	010001 1110
D30.6	110 11110	011110 0110	100001 0110	D30.7	111 11110	011110 0001	100001 1110
D31.6	110 11111	101011 0110	010100 0110	D31.7	111 11111	101011 0001	010100 1110

Table B-3 displays the full valid special character 8B/10B codes.

Table B-3. Valid Special Characters

Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdie fghj
K28.0	000 11100	001111 0100	110000 1011	K28.6	110 11100	001111 0110	110000 1001
K28.1	001 11100	001111 1001	110000 0110	K28.7	111 11100	001111 1000	110000 0111
K28.2	010 11100	001111 0101	110000 1010	K23.7	111 10111	111010 1000	000101 0111
K28.3	011 11100	001111 0011	110000 1100	K27.7	111 11011	110110 1000	001001 0111
K28.4	100 11100	001111 0010	110000 1101	K29.7	111 11101	101110 1000	010001 0111
K28.5	101 11100	001111 1010	110000 0101	K30.7	111 11110	011110 1000	100001 0111

Appendix C
Revision History

This appendix provides a list of the major differences between revisions of the *MC92603 Quad Gigabit Ethernet Transceiver Reference Manual* (MC92603RM).

Table C-1 provides a revision history for this document.

Table C-1. Revision History Table

Document Revision	Substantive Changes
Rev 0	Initial release
Rev 1	Reformatted to Freescale with minor edits. Added last paragraph on internal service termination to Section 3.4, “Receiver Interface Configuration.” Changed values in Table 8-1, "MC92603 Package Thermal Resistance Values.

Glossary of Terms and Abbreviations

The glossary contains an alphabetical list of terms, phrases, and abbreviations used in this book. Some of the terms and definitions included in the glossary are reprinted from IEEE Std 754-1985, *IEEE Standard for Binary Floating-Point Arithmetic*, copyright ©1985 by the Institute of Electrical and Electronics Engineers, Inc., with the permission of the IEEE.

A

Asserted. Indicates active state of signal has been set. Refers to either inputs or outputs.

B

BERC. Bit Error Rate Checking.

BERT. Bit Error Rate Testing.

BIST. Built-In Self-Test.

Bit alignment. Refers to the transition tracking loop recovering data bits from the serial input stream.

Byte. Eight bits of uncoded data.

Byte alignment. Receiver identification of character boundaries through use of Idle character recognition.

C

Character. An 8B/10B encoded byte of data.

D

Double data rate (DDR). The data is transferred on both the rising and falling edge of the clock rather than on just the rising edge.

G

Gigabit. A unit of speed of data transfer. One gigabit indicates a data throughput of 1 billion bits per second requiring a transfer rate of 1.25 billion symbols per second of 8B/10B encoded data.

Gigabaud. A unit of speed of symbol transfer. One gigabaud indicates a data throughput of 800 million bits per second requiring a transfer rate of 1.0 billion symbols per second of 8B/10B encoded data.

Gigabit media independent interface (**GMII**). The interface between the reconciliation sublayer and the physical coding sublayer (PCS) for a 100 Mbps operation.

I

Inter-packet gap (**IPG**). The delay or time gap in between CSMA/CD packets. The delay provides interframe recovery time for other CSMA/CD sublayers and for the physical medium.

Inter Symbol Interference (**ISI**). A distortion caused by the high-frequency loss characteristics of the transmission media.

L **Least-significant bit** (**lsb**). The bit of the least value in an address, register, data element, or instruction encoding.

M **Media access controller (MAC)**. The data link sublayer that is responsible for transferring data to and from the physical layer.

N **Negated**. Indicates inactive state of signal has been set. Refers to either inputs or outputs.

P **Physical coding sublayer** (**PCS**). PCS is defined as part of a sublayer in the IEEE Std. 802.3-2002 [4]. The PCS sublayer encodes data bits into code-groups that can be transmitted over the physical medium. It is used to couple the gigabit media independent interface (GMII) and a physical medium attachment (PMA).

Phase Locked Loop (**PLL**).

Physical medium attachment (**PMA**) sublayer. The PMA is defined as part of a sublayer in the IEEE Std. 802.3-2002 [4]. The PMA is part of the physical layer that provides transmission, reception, collision detection, clock recovery, and skew alignment.

Parts per million (**ppm**).

R **Reduced Gigabit Media Independent Interface** (**RGMII**). The reduced interface between the reconciliation sublayer and the physical coding sublayer (PCS). The interface is reduced from 8-bit wide to 4-bit wide and data transfer is DDR.

Reduced Ten Bit Interface (RTBI). The reduced interface between the reconciliation sublayer and the physical coding sublayer (PCS).The interface is reduced from 10-bit wide to 5-bit wide and data transfer is DDR.

Running disparity. The amount of DC imbalance over a history of symbols transmitted over a link. Equal to the difference between the number of one and zero symbols transmitted.

S **SerDes**. Serializer/deserializer.

Symbol. One piece of information sent across the link; different from a bit in that bit implies data where symbol is encoded data.

T **Ten bit interface physical layer** (**TBI PHY**) interface.

W **Word synchronization**. Alignment of two or more receivers' data by adjusting for differences in media and systemic delay between them such that data is presented by the receivers in the same grouping as they were transmit.

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